ISSN: 2449 - 0539
BAYERO JOURNAL OF ENGINEERING AND TECHNOLOGY VOL 18 NO. 2 MAY 2023 PP. 19-27

EXPERIMENTAL VOLTAGE BALANCING BASED SORTING ALGORITHM FOR MODULAR MULTILEVEL CONVERTERS

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ABSTRACT

Of paramount importance to the proper operation of modular multilevel converter (MMC) is the sub-module (SM) capacitor voltage balancing. Two major approaches proposed to achieve this task are distributed method and centralized method. This paper presents an experimental implementation of the centralized SM capacitor voltage balancing control strategy in MMC based on sorting algorithm. The concept was experimentally demonstrated on a laboratory prototype MMC with four SMs per arm. The results show that the SM capacitor voltages are properly balanced and regulated to their reference values. Furthermore, the resultant output voltage and current waveforms exhibit perfect harmonic performance with fundamental switching frequency; thus confirming the effectiveness of the control method.

Keywords: Modular multilevel converter (MMC); sub-module (SM); sorting algorithm; capacitor voltage balancing (CVB), sub-module capacitor voltage.

1. INTRODUCTION

The modular multilevel converter (MMC) has been a subject of hot research in the field of high voltage direct current (HVDC) transmission system, medium and high voltage motor drives, grid integration of large scale solar and wind energy conversions system (WECS) and flexible alternating current transmission system (FACTS) devices (Kadandani, Dahidah, & Ethni, 2021). The MMC combines the advantages of having low switching losses, distributed location of capacitor voltage, simple capacitor voltage balancing control (CVB), fault tolerant operation, simple realization of redundancy, low harmonic distortion, as well as scalability to higher voltage and power levels, less semiconductor stress and easy component assembling (Kadandani, Dahidah, & Ethni, 2019).

For the converter to operate properly, a lot of parameters need to be controlled properly. For example, the sub-module (SM) capacitor voltages, energy across the upper and lower arms, energy across the converter legs, circulating current through the converter arms, and the temperature across the converter SMs need to be controlled. Among all these parameters, the voltage balancing across the converter SMs is the most essential (Ilves, Harnefors, Norrga, & Nee, 2015). Two methods have been proposed in the literature to balance the SM capacitor voltages in MMC: distributed method and centralized method (Fan, Zhang, Xiong, & Xue, 2015). The former involves a complex control architecture with a separate closed loop control for each SM (Hagiwara, Maeda, & Akagi, 2011) while the later

takes into account the SM capacitor voltages and arm current polarities to select certain SMs for certain switching states (Saeedifard & Iravani, 2010).

The objective of this paper is to experimentally demonstrate the sorting algorithm based SM capacitor voltage balancing strategy on a reduced scale laboratory MMC prototype. The concept is demonstrated on an MMC with only four SMs per arm in order to prevent high switching frequency of the converter semiconductor devices and to reduce excessive computational cost.

The paper is organised as follows. In Section 2, the concept of MMC is presented. The details of the sorting algorithm based SM capacitor voltage balancing strategy is presented in Section 3. Experimental results are presented in Section 4. The conclusion drawn from the paper are summarized in Section 5.

2. THE MODULAR MULTILEVEL CONVERTER

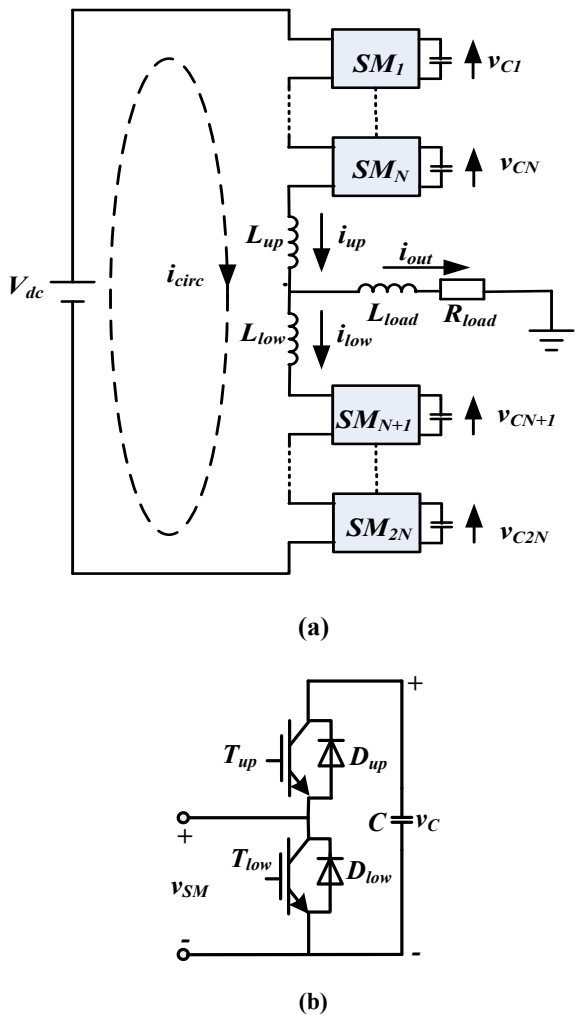


Figure 1: Circuit schematic of 1 phase of MMC, **(a)** Circuit configuration, **(b)** Bidirectional HBSM chopper cell

Figure 1(a) shows the circuit schematic of one phase leg of MMC. The phase leg consists of two arms; upper and lower. Each arm consists of *N* number of bidirectional SMs, and an arm inductor, *L* which is used to suppress the DC fault current within each phase leg of the converter and also to limit the circulating current. In the figure, V_{dc} is the input DC voltage, L_{arm} and $R_{arm,}$ are the arm inductance and its resistance, i_{up} and i_{low} are the currents through the upper and lower arm respectively, i_{circ} is the circulating current, L_{load} and R_{load} represents an RL load, i_{ac} and v_{ac} are the output AC current and voltage respectively, v_{SM} is the SM voltage, C is the SM capacitor and v_C is the SM capacitor voltage.

Figure 1(b) shows a circuit schematic of half bridge SM (HBSM) in which T_{up} and D_{up} are the IGBT and diode in the upper module while T_{low} and D_{low} are the IGBT and diode in the lower module, i_{SM} and v_{SM} are the current and voltage of the SM, C is the SM capacitor and v_C is the SM capacitor voltage. When an SM is activated, its output voltage assumes the value of its capacitor voltage ($v_{SM} = v_C$). On the contrary, when an SM is deactivated, it will act as short circuit and its output voltage will be zero ($v_{SM} = 0$). During operation, SMs are continuously activated and deactivated and their values are added to yield the desired multilevel arm voltage.

If $S(k)$ is the switching state of *kth* SM, then the total voltage across the upper and lower arm, v_{up} and v_{low} can

be expressed as (N.B. Kadandani, 2021):

$$v_{up} = \sum_{x=1}^{N} S_{up}(k) \,.\, v_{C\_up}(k) \quad (1)$$

$$v_{low} = \sum_{x=N+1}^{2N} S_{low}(k) \,.\, v_{C\_low}(k) \quad (2)$$

Table 1 gives a summary of the three modes of operation of SM, namely; insertion, bypassing and blocking modes.

Table 1: Operational modes of HBSM in MMC

State	Mode	Switching state		i_{SM}	v_{SM}	Conducting device	Capacitor state
		T_{up}	T_{low}				
1	Insertion	ON	OFF	> 0	v_C	D_{up}	Charging
2		ON	OFF	< 0	v_C	T_{up}	Discharging
3	Bypassing	OFF	ON	> 0	0	T_{low}	Bypassed
4		OFF	ON	< 0	0	D_{low}	Bypassed
5	Blocking	OFF	OFF	> 0	v_C	D_{up}	Charging
6		OFF	OFF	< 0	0	D_{low}	Bypassed

3. CAPACITOR VOLTAGE BALANCING FOR MMC

In MMC, capacitor voltage balancing (CVB) is a major requirement in order to achieve equal power distribution among the SMs. Several methods have been proposed to address CVB with the common ones being distributed and centralized methods (Fan et al., 2015).

3.1. Distributed Method

As proposed in (Hagiwara & Akagi, 2008; Hagiwara, Maeda, & Akagi, 2010; Li, Li, Williams, & Xu, 2016), the distributed method employs carrier phase-shifted pulse-width modulation (CPS-PWM) in a closed-loop control to balance the capacitor voltage to its reference value. It is worth noting that CVB based on distributed method is achieved with some modification on the modulating signal. However, it results in good balancing at higher switching frequencies.

The approach consists of one or combination of three cascaded control loops; averaging control, arm balancing control and individual capacitor voltage balancing control. The averaging control is meant to force the average capacitor voltage from the phase leg to follow its reference value. The arm balancing control is meant to mitigate the voltage dif-

ference that may exist between the average of the upper and lower arm voltages. The individual balancing control is required in order to force the individual capacitor voltage in each module to follow its reference value.

A block diagram of a simple distributed method of capacitor voltage balancing considering arm balancing is shown in Figure 2 where v_m is the modulation voltage, i_{up} and i_{low} are the upper and lower arm current respectively, $\overline{v_{C\_up}}$ and $\overline{v_{C\_low}}$ are the average capacitor voltage in upper arm and lower arm respectively, and v_{Ck} (k: 1~2N; N being the number of SMs per arm) is the capacitor voltage of the individual SMs.

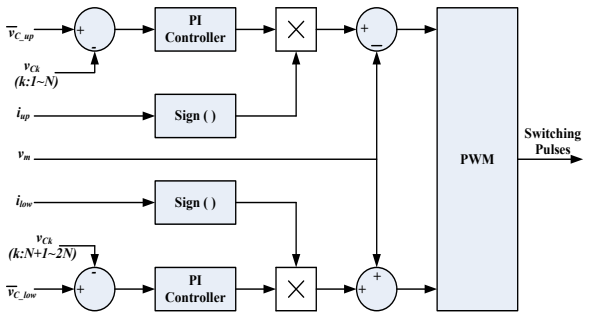


Figure 2: Block diagram of a typical distributed method of capacitor voltage balancing

3.2. Centralized Method

This method was proposed in (Li et al, 2016; Dekka, Wu, Zargari, & Fuentes, 2016; Lesnicar & R.Marquardt, 2003; Rohner, Bernet, Hiller, & Sommer, 2010; Siemaszko, 2015; and Wang, Li, Zheng, & Xu, 2013). It makes use of SM capacitor voltages and arm current polarities to select certain SMs for certain switching states. The modulation involves measuring and sorting SM capacitor voltages within an arm for every PWM period. In this process, the SMs with lowest capacitor voltages are activated when the arm current is positive. This will enable the SM capacitors to be charged and increase their voltages. Conversely, the SMs with highest capacitor voltages are activated when the arm current is negative, in this case, the SM capacitors are discharged and their voltages decreased.

A block diagram of a typical centralized method of CVB is shown in Figure 3 where v_C is the SM capacitor voltage, i_{arm} is the arm current, i_{up} and i_{low} are the upper and lower arm current respectively.

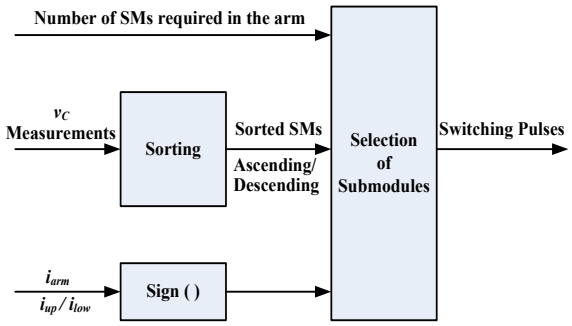


Figure 3: Block diagram of a typical centralized method of capacitor voltage balancing

4. EXPERIMENTAL IMPLEMENTATION

4.1. Experimental Set-up

As shown in Figure 4, the experimental set-up is based on a single phase laboratory prototype MMC with 4 SMs per arm implemented with system parameters of Table 2.

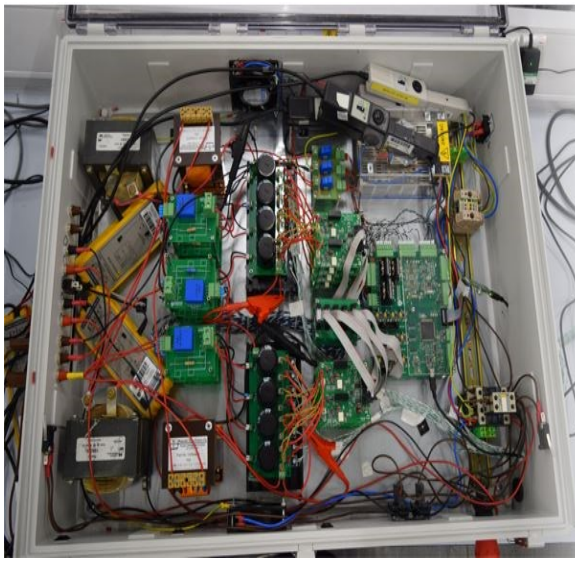
The coding for the *sorting algorithm based CVB* is based on the following procedure:

- Measuring the capacitor voltage of each SM in the converter arm and sort them in ascending or descending order

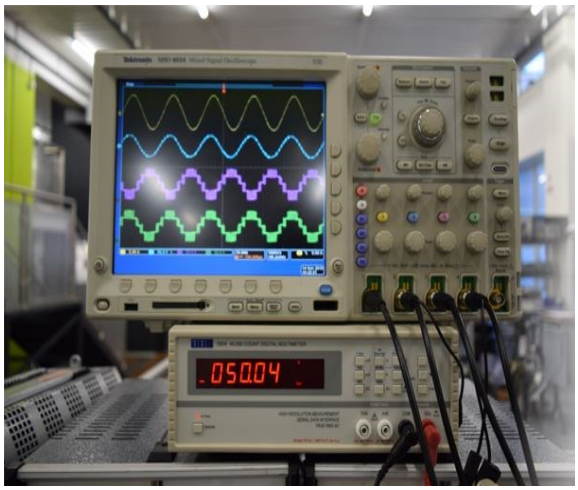
- Monitoring the direction of the arm current and acquiring the number of SMs that need to be inserted
- Selecting the required number of SMs that need to be switched on based on the direction of the arm current and the sorted voltage sequence
- When the arm current is positive, the SMs with lowest voltage are switched on (inserted), so that their capacitors are charged and their voltage increase
- When the arm current is negative, the SMs with highest voltage are switched on (inserted), so that their capacitors are discharged and their voltage decrease
- For any bypassed SM, its voltage remained unchanged. Accordingly, the capacitor voltages are relatively kept balanced
- This pattern continues until the voltage reference have been achieved.

Table 2: Parameters of the experimental set-up

Parameter	Value
Number of submodule per arm	4
Submodule capacitance	4.7mF
Reference capacitor voltage	25V
Arm inductance	1mH
Load resistor	5Ω
Load inductor	4mH
DC link voltage	100V
Output AC voltage reference	50V
Carrier frequency	4kHz
Modulation index	0.9



(a)



(b)

Figure 4: Experimental set-up, **(a)** MMC test rig prototype, **(b)** Oscilloscope reading

Figure 5 gives an illustration of the sorting algorithm when the direction of the arm current is positive. It represents a case for the four SM laboratory prototype MMC used in the research. The upper box in the figure represents the four SM voltages being measured. The middle box represents the sorted voltage sequence in ascending order employing bub-

ble sort. The lower box represents the selected voltage whose SMs would be inserted (smallest ones). The reverse (higher ones) will be the case if the direction of the arm current is negative

Capacitor voltage index	v_{c1}	v_{c2}	v_{c3}	v_{c4}
Capacitor voltage value	**24.9**	**24.8**	**25.2**	**25.1**

Sorting the SM ☐ capacitor voltages

Capacitor voltage index	v_{c2}	v_{c1}	v_{c4}	v_{c3}
Capacitor voltage value	**24.8**	**24.9**	**25.1**	**25.2**

Selecting the smallest ☐ to insert their SMs

Capacitor voltage index	v_{c2}	v_{c1}	v_{c4}	v_{c3}
Capacitor voltage value	**24.8**	**24.9**	**25.1**	**25.2**

Figure 5: Illustration of the sorting algorithm for capacitor voltage balancing in MMC

4.2. Results and Discussion

Figure 6 through 11 show the results obtained from the sorting algorithm based CVB in the four SMs laboratory prototype MMC.

Figure 6 and 7 show the SM capacitor voltages for the upper and lower arm of the converter. In both figures, the SM capacitor voltages are balanced and regulated to the reference value by the sorting algorithm based CVB. Also, the harmonics in individual SM capacitor voltages are significantly reduced. This confirms the effectiveness of the sorting algorithm based CVB control strategy.

Figure 8 shows the multilevel arm voltages (for the upper and lower arms) of the converter. The voltages exhibit clear staircase waveforms also with minimum harmonic component.

Figure 9 shows the output voltage waveform which is nearly sinusoidal in shape. The harmonic contents in the output waveform is very negligible, thus confirming the effectiveness of the control method.

Figure 10 shows the current waveforms in the upper and lower arms of the converter. The arm current waveforms does have second order harmonic component due to inherent circulating current in the converter. Incidentally, circulating current control is not considered in this paper. However, different methods of circulating current control have been presented in (Kadandani, Dahidah, & Ethni, 2021) Researches in (Kadandani, Dahidah, Ethni, & Muhammad, 2021) have considered circulating current control as a means of improving the lifetime and reliability of MMC.

Figure 11 shows the output current waveform of the converter which seems to be smooth sinusoidal in shape. Fortunately, the circulating current does not affect the output current waveform.

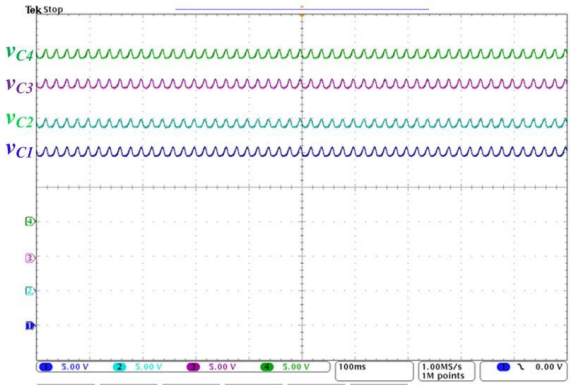


Figure 6: Upper arm capacitor voltage waveforms of the converter

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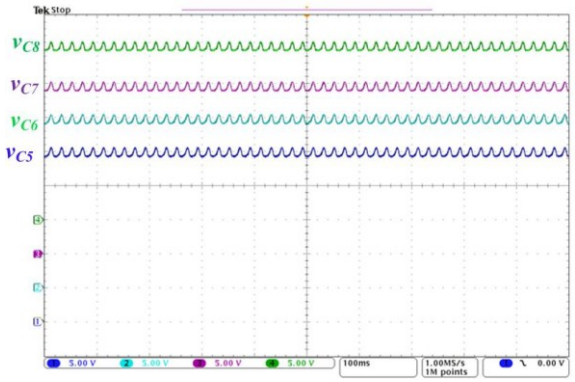

Figure 7: Lower arm capacitor voltage waveforms of the converter

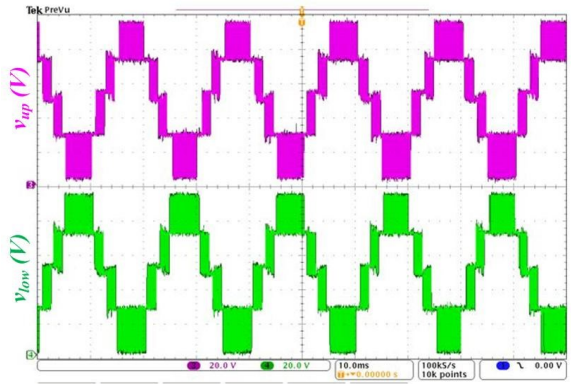

Figure 8: Upper and lower arm voltage waveforms of the converter

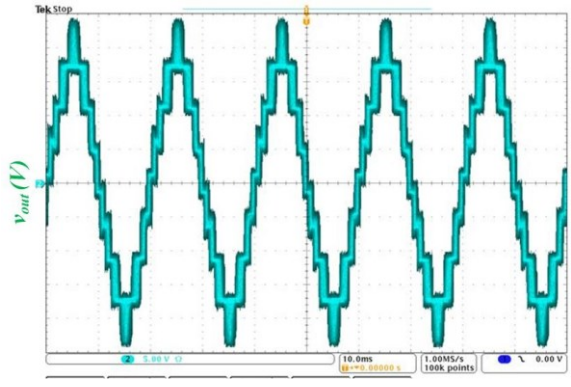

Figure 9: Output voltage waveform of the converter

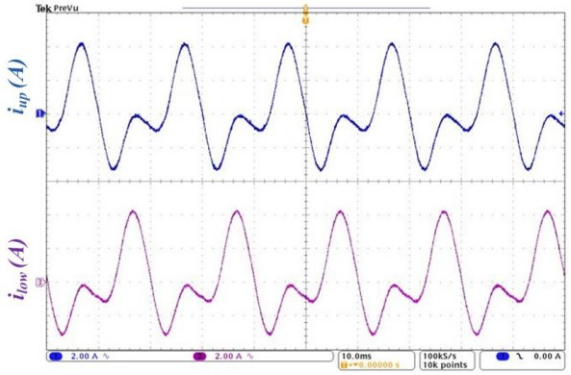

Figure 10: Upper and lower arm current waveforms of the converter

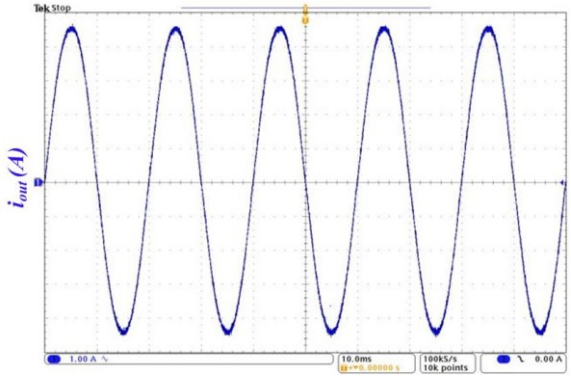

Figure 11: Output current waveform of the converter

5. CONCLUSION

In this paper, an experimental implementation of sorting algorithm based capacitor voltage balancing strategy for MMC is presented. The algorithm is demonstrated on a laboratory prototype MMC with four SMs per arm. The results show that the SM capacitor voltages are properly balanced and regulated to their reference value. The current and voltage waveforms obtained are of reduced harmonic content and nearly sinusoidal in shape.

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