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EXPERIMENTAL IMPLEMENTATION OF CARRIER PHASE SHIFT PULSE WIDTH MODULATION TECHNIQUE IN MODULAR MULTILEVEL CONVERTER

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ABSTRACT

The modular multilevel converter (MMC) is an emerging and highly efficient voltage source converter (VSC) topology for medium and high voltage applications. The converter has multivariable that need to be controlled for proper operation of the converter. All the MMC control loops are linked to the modulation voltage synthesis for providing appropriate gate signals for the converter switches. Different modulation techniques have been proposed to obtain appropriate switching pulses. The most common ones being stair case modulation and carrier phase shift pulse width modulation (CPS-PWM) techniques. This paper presents an experimental implementation of CPS-PWM in MMC which is the most suitable and recommended modulation technique for small and medium scale MMC with reduced number of submodules (SMs). The concept is experimentally demonstrated on an MMC with three SMs per arm. The results show perfect harmonic performance with fundamental switching frequency.

Keywords: Carrier phase shift pulse width modulation (CPS-PWM), modular multilevel converter (MMC), submodule (SM), modulation technique.

1. INTRODUCTION

Modern wind energy conversion system (WECS), large scale solar power systems, high voltage direct current transmission systems (HVDC), traction system, medium and high power motor drives have adopted voltage source converters (VSCs) technology in the last two decade. However, among all the VSCs used in these applications, the MMC topology is becoming more popularised due to its high modularity, low distortion, high efficiency, high reliability, lower switching losses and reduced EMI noise (Kadandani et al, 2021). For example, the work reported in (Rong et al, 2019) employs MMC in WECS for control strategy under asymmetrical grid faults. In similar development, (Basu & Maiti, 2019) employs hybrid MMC in solar power integration. In (Dey & Bhattacharya, 2021) however, a transformerless DC–DC MMC is proposed for hybrid interconnections in HVDC transmission system. In another development, (He et al, 2019) proposed a novel advanced power supply system based on MMC for modern traction application while (Zhao et al., 2020), proposed a coordinated strategy of low-speed and start-up operation for medium-voltage variable-speed drives with MMC. In another development, (Diab et al, 2020) proposed MMC STATCOM for improving power quality indicators.

MMC has many parameters that need to be controlled for proper operation of the converter. These control aspects include capacitor voltage balancing, circulating current control, output voltage control and output current control. These control loops are then linked to the modulation voltage synthesis for providing pulse width modulation (PWM) signals required to trigger the semiconductor switches in the converter SMs. Different modulation techniques have been proposed in the literature to fit the MMC. The modulation techniques dedicated for MMC are divided into two major classes; space vector based techniques and voltage level based techniques.

The space vector modulation (SVM) algorithm as demonstrated in (Ronaki & Williamson, 2019) is based on representing the reference voltage in the alpha-beta plane as a vector to be generated by the converter. Depending on the control strategy, the SVM technique can be classified into two dimensional SVM (2D-SVM) or three dimensional SVM (3D-SVM). In the case of 2D-SVM, the output voltage level is synthesised from the switching states of the converter and the voltage reference vector is generated as linear combination of multiple vectors at every sampling period (Kadandani, 2021). As such, the 2D-SVM is for control strategy involving a balanced system that is free of triple harmonics. The 3D-SVM was implemented in (Schuetz, Carnielutti, Pinheiro, &

Grigoletto, 2019). It is typically applied for unbalanced system as well as in system with or without neutral and is employed when the control algorithm is designed to control zero sequence or triple harmonics.

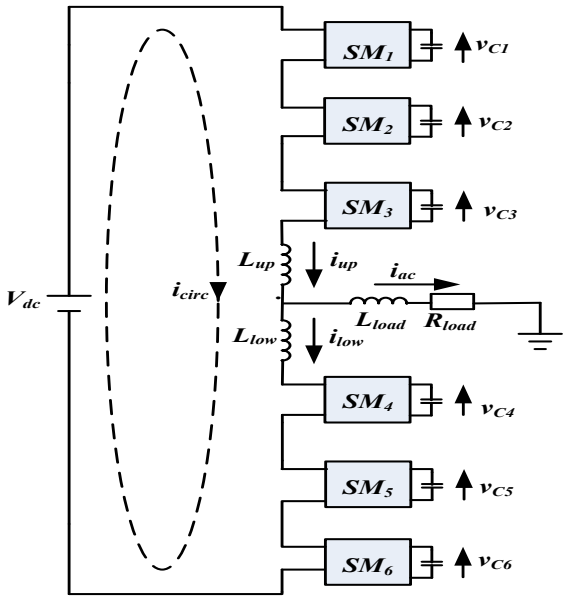
The voltage level based modulation techniques include nearest level modulation (NLM), selective harmonic elimination (SHE), hybrid modulation (HM), level shifted PWM (LS-PWM) and carrier phase shifted PWM (CPS-PWM). The NLM technique is reported in (Wang et al., 2018) and it is based on an approximation such that the voltage levels which are nearest to the reference values are chosen for modulation. In other words, NLM technique generates the voltage level that is closest to voltage reference for full switching period. The SHE technique as implemented in (Haghdar & Shayanfar, 2018) is based on calculating the switching angles required for the cancellation of some selected harmonics. In other words, SHE modulation technique is meant to cancel out low frequency harmonics and improve the THD of the output voltage. In the case of LS-PWM, multicarrier signals are arranged with defined shifts in amplitude such that each carrier is related with an output voltage level being generated by the converter. A Study of LS- PWM single-phase 11-level multilevel inverter was presented in (Hassan et al, 2019). In this technique, N carrier signals are distributed vertically along the modulating signal and the modulating signal is compared with each carrier for the activation of SMs. The CPS-PWM technique is based on assigning one carrier for each individual SM that is to be modulated. The N carriers have the same frequency but are phase shifted by $360^{o}/N$ in order to generate a multilevel output voltage with minimum harmonic content (Kadandani, 2021). A detail analysis and operation of MMCs with CPS-PWM was presented in (Ilves et al, 2015) while a more generalized theory of the CPS-PWM technique for cascaded H-bridge converters and MMCs was presented in (Li, Wang, & Li, 2016). This paper therefore presents a hardware implementation of the CPS-PWM in a small-scale laboratory MMC prototype of single phase with three SMs per arm.

The remaining parts of this article is organised as follows. Section 2 presents the theoretical background and mode of operation of MMC. Section 3 presents a detail analysis of the CPS-PWM technique in MMC with some illustration on the experimental prototype of MMC with three SM per arm. In section 4, an experimental implementation of the CPS-PWM in a single phase MMC with three SMs per arm is presented. Lastly, section 5 concluded the article.

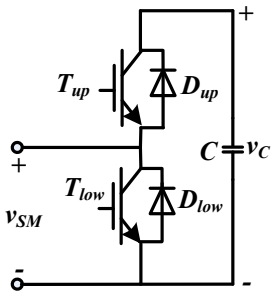
2. MODULAR MULTILEVEL CONVERTER TOPOLOGY AND WORKING PRINCIPLES

2.1. Modular Multilevel Converter Topology

Figure 1 shows the circuit topology of one phase of MMC. It consists of two identical arms; upper and lower each of which is connected to an arm inductor. Each arm consists of series connected chopper cells known as submodules (SM). During normal operation, a SM can either be inserted or bypassed. When inserted, a SM output its capacitor voltage whereas when bypassed, its output is zero. An SM can be configured in one of the following: half bridge SM (HBSM), full bridge SM (FBSM), flying capacitor SM (FCSM), diode clamped SM (DCSM), T-Submodule 1 (TSM1) or T-Submodule 2 (TSM2). In this work, HBSM is used because of its simplicity in terms of component count, lowest losses and easy control method.



(a)



(b)

Figure 1: Circuit topology of one phase of MMC, (a) Topology configuration, (b) Half bridge SM

2.2. HBSM and its Mode of Operation

An HBSM is made up of DC capacitor, C and two semiconductor switches that insert or bypass the capacitor in series within the arm. Fig. 1(b) shows a circuit schematic of HBSM in which T_{up} and D_{up} are the IGBT and diode in the upper module while T_{low} and D_{low} are the IGBT and diode in the lower module, i_{SM} and v_{SM} are the current and voltage of the SM, C is the SM capacitor and v_C is the SM capacitor voltage. When an SM is activated, its output voltage assumes the value of its capacitor voltage ($v_{SM} = v_C$). On the contrary, when an SM is deactivated, it will act as short circuit and its output voltage will be zero ($v_{SM} = 0$). During operation, SMs are continuously activated and deactivated and their values are added to yield the desired multilevel arm voltage.

During operation, an SM toggles between on-state and off-state. During the on-state, the terminal voltage of the SM is zero, whereas during the off-state, the voltage assumes the value of its module capacitor, v_C (DC energy storage of the SM). In other words, the state of the SM shown in Figure 1(b) is said to be switched-on if T_{up} is switched ON and T_{low} is switched OFF; in which case, the voltage v_{SM} equals v_C. In contrast, the SM state is said to be switched-off if T_{up} is switched OFF and T_{low} is switched ON; in which case, the v_{SM} is zero. Table 1 summarised the switching state of SM for the proper operation of the MMC.

Table 1: Switching states of SM during MMC operation

SM State	T_{up}	T_{low}	v_{SM}
On	On	Off	v_C
Off	Off	On	0

The switching sequence of upper and lower arms are complementary. The output of the series connected SMs are combined to generate appropriate multilevel arm voltage; namely upper arm voltage v_{up} and lower arm voltage v_{low}. The DC capacitor of an SM can either contribute to the output voltage or be bypassed, hence, v_{up} and v_{low} collaborate to yield the desired output AC voltage v_{ac}. The sum of v_{up} and v_{low} is equal to the value of the DC link voltage V_{dc}. This implies that the AC and DC sides of the converter can be independently controlled.

3. CARRIER PHASE SHIFT PULSE WIDTH MODULATION TECHNIQUE FOR MMC

The main purpose of the modulator is to synthesise the AC waveform by activating SMs. Each arm of the converter has its own modulator that works independently. Each modulator works in hand with voltage balancing controller in selecting and activating an SM. The output of the modulation in any arm is a multilevel pulse waveform. Figure 2 shows the classification of modulation techniques in MMC.

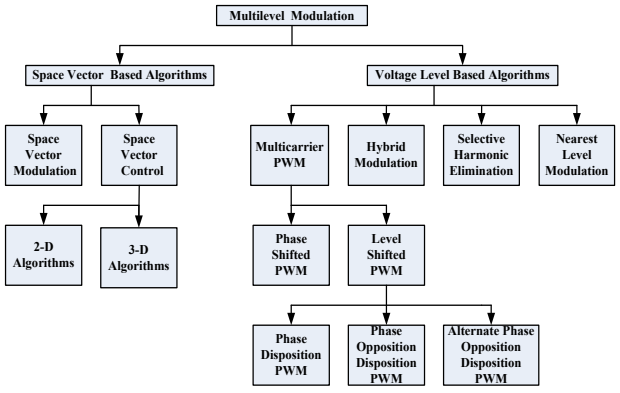


Figure 2: Modulation techniques in MMC

Figure 3 shows the schematic of CPS-PWM in one arm of MMC. In particular, the schematic represent the case of a converter with three SMs per arm as experimented in this research. As such, there are three carrier

signals (v_{cr_1}, v_{cr_2} and v_{cr_3}) and a modulating signal, v_m. Each carrier signal correspond to one SM. In other words, the number of carrier signals is equal to the number of SMs. In order to achieve proper harmonic cancellation in a converter with N number of SMs per arm, the phase shift between any two adjacent carriers has to be equal to 2π/N (Wang & Tang, 2019). CPS-PWM provides good output voltage performance in MMC with limited SMs (Debnath et al, 2015).

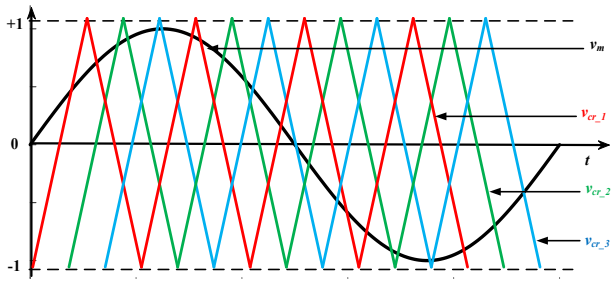


Figure 3: CPS-PWM in one arm of MMC

The equivalent switching frequency of the converter, f_{eq} is given by:

$$f_{eq} = Nf_{cr} \quad (1)$$

where f_{cr} is the carrier frequency.

The CPS-PWM technique provides equal conduction times for all the SMs (Kadandani, 2021).

The control technique was built in two cascaded control loops; average DC voltage control and individual DC voltage control. Figure 4 shows the block diagram of the control strategy.

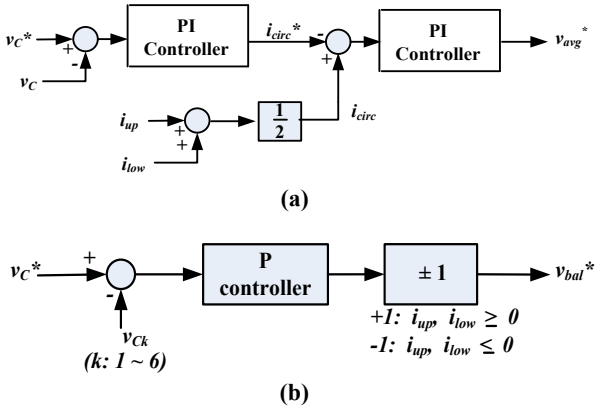


Figure 4: MMC Control Strategy,

The average DC voltage control shown in Figure 4(a) is meant to force the average DC capacitor voltage of each phase to follow its reference value. This control algorithm is based on comparing the average capacitor voltage, $\overline{v_C}$ with its reference value, v_C^*. Based on this, two proportional-integral (PI) controllers are designed to give the required reference averaging voltage command, v_{avg}^*. The resulting reference averaging voltage commands, v_{avg}^* is then used as a component in generating the reference modulating signal for sending appropriate switching signals to the converter semiconductor switches.

The individual DC voltage control shown in Figure 4(b) is to force the DC capacitor voltages of individual SMs to follow the reference value. This control algorithm is based on comparing each individual capacitor voltage, v_{Ck} (k: 1~2N; N being the number of SMs per arm) with the reference value, v_C^* and with a proportional (P) controller that will yield a reference balancing voltage command, v_{bal}^* depending on the polarity of the current in the upper arm, i_{up} or that of the lower arm, i_{low}. The resulting reference balancing voltage command, v_{bal}^* is then used as another component in generating the reference modulating signal for sending appropriate switching signals to the converter semiconductor switches.

The voltage commands for each SM in the upper arm is given by:

$$v_k^* = v_{avg}^* + v_{bal}^* - \frac{v_{ac}^*}{N} + \frac{V_{dc}}{2N}, \quad (k = 1{:}N) \quad (2)$$

While the voltage commands for each SM in the lower arm is given by:

$$v_k^* = v_{avg}^* + v_{bal}^* + \frac{v_{ac}^*}{N} + \frac{V_{dc}}{2N}, (k = N+1{:}2N) \quad (3)$$

The value of v_k^* in each SM is normalized by the SM capacitor voltage, v_{Ck}. Each of the resulting modulating signals were individually compared with carrier signals

of switching frequency, f_{cr}. To enhance current controllability and ensure harmonic cancellation, the carrier waveforms of the SM cells were phase shifted by 360°/N. Accordingly, multilevel voltage waveform with $N+1$ levels are obtained at each arm of the converter.

4. EXPERIMENTAL IMPLEMENTATION

4.1. Experimental Set-up

The experimental prototype is implemented based on the parameter values of Table 2 and is illustrated in Figure 5. The MMC prototype is a single phase converter with 3 SMs per arm. The set-up has seven voltage sensors (for measuring the 6 SM voltages and the output voltage) and three current sensors (for measuring the two arm currents and the output current). The CPS-PWM control technique was implemented experimentally using Texas Instrument TMSF28377D Dual-Core Delfino™ microcontroller board with code composer studio. Figure 6 shows the communication structure of the experimental set-up.

Table 2: Parameters of the experimental set-up

Parameter	Value
Number of submodules per arm	3
Submodule capacitance	2.2mF
Arm inductance	1mH
Load resistor	33Ω
Load inductor	1mH
DC link voltage	100V
Carrier frequency	4kHz
Modulation index	0.9

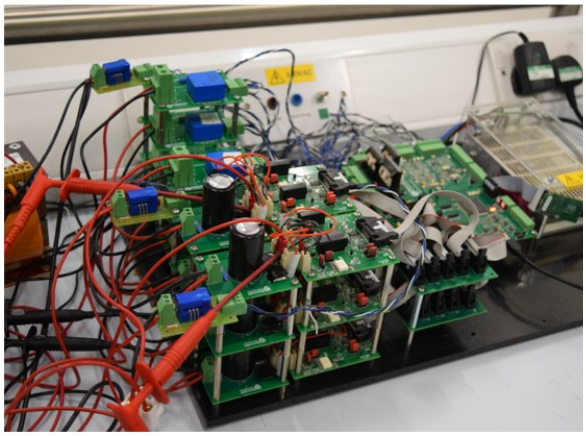


Figure 5: Photograph of the experimental platform

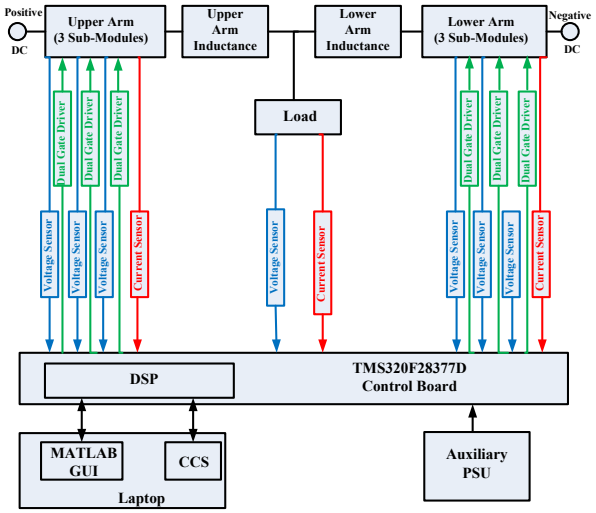
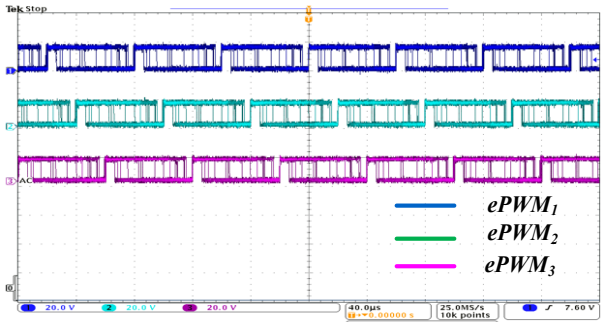


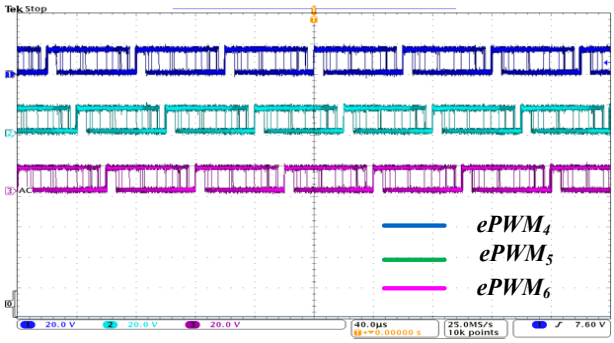
Figure 6: Communication structure of the experimental set-up

4.2. Results and Discussion

Figure 7 through 12 show the waveforms obtained from the CPS-PWM control strategy implemented on the three SM laboratory prototype MMC system.



(a)



(b)

Figure 7: Enhanced PWM, (a) Upper arm, (b) Lower arm

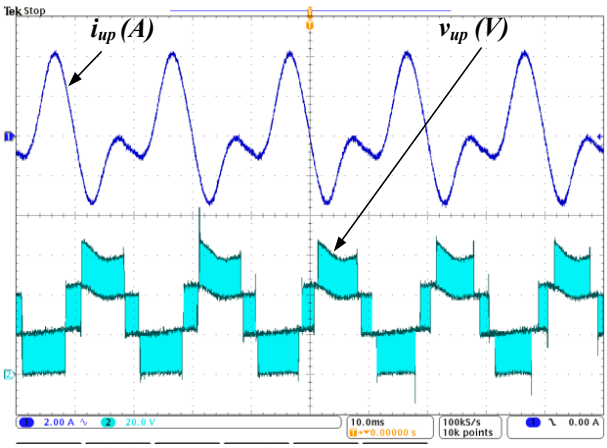


Figure 8: Current and voltage waveform in upper arm of the converter

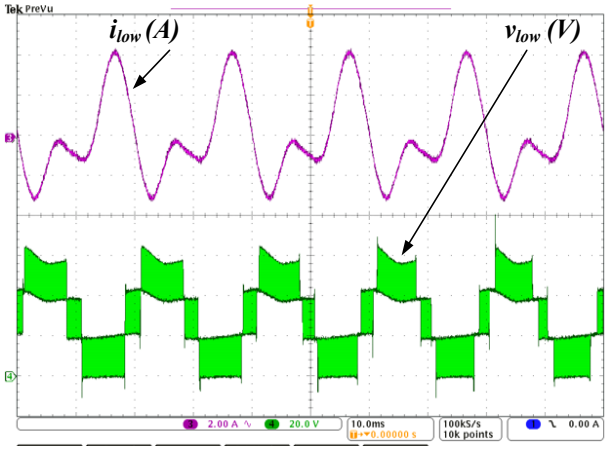


Figure 9: Current and voltage waveform in lower arm of the converter

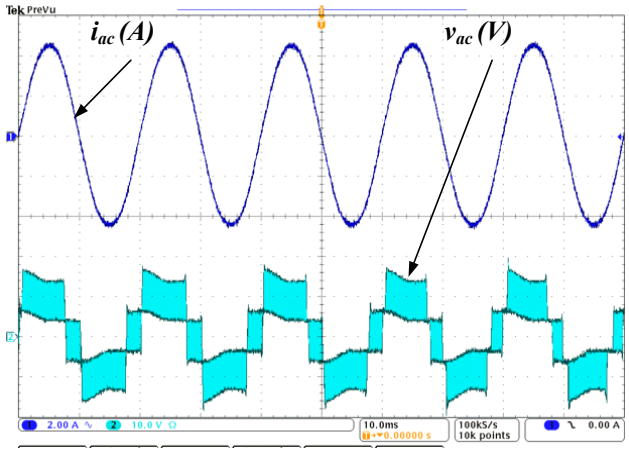


Figure 10: Current and voltage waveform at the output of the converter

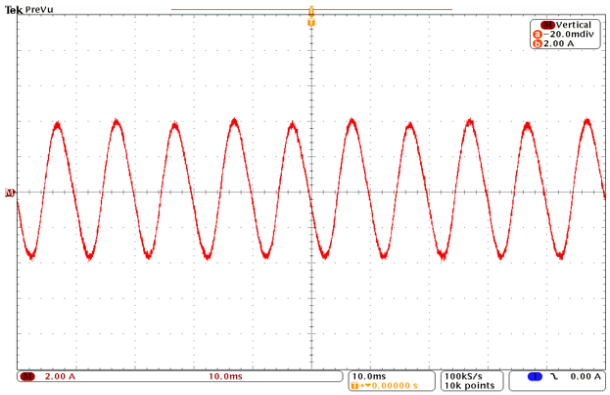


Figure 11: Circulating current

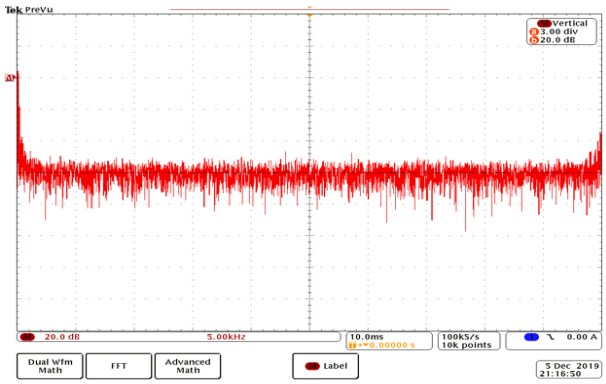


Figure 12: FFT analysis on the circulating current

Figure 7 shows the enhanced PWM signals (ePWM) of the converter. Figure 7(a) represents the upper arm ePWM signals while figure 7(b) shows that of lower arm. It can be seen from both figures that the six ePWM signals have a phase shift of 60° (=360°/6) to each other. This is a clear sign of harmonic reduction required for enhanced current controllability.

Figure 8 shows the current and multilevel arm voltage in the upper arm while Figure 9 shows similar waveforms in lower arm. In both figures, the arm currents show harmonic component due to the presence uncontrolled circulating current in the converter. Incidentally, circulating current is an inherent feature of MMC and therefore needs a dedicated control algorithm for its suppression. On the other hand, the multilevel arm voltages in both figures shows clear staircase voltage waveform with reduced harmonic component.

Figure 10 shows the current and voltage waveforms at the output of the converter. Both waveforms show perfect harmonic performance with fundamental switching frequency and improved power quality. Figure 11 shows the circulating current in the converter while figure 12 shows the First Fourier Transform (FFT) analysis on the circulating current. The circulating current in MMC arises from inner voltage differences among each phase unit of the converter. It usually manifests itself in the form of second order harmonics on the arm currents of the converter. However, circulating current can be controlled to enable proper operation of the converter. Circulating current control (CCC) is outside the scope of this article but several CCC methods are extensively reviewed in (Kadandani, Dahidah, & Ethni, 2021).

5. CONCLUSION

This paper demonstrated carrier phase shift pulse width modulation technique on a laboratory prototype modular multilevel converter with three submodules per arm. The technique was implemented alongside a distributed method of capacitor voltage balancing control consisting of average DC voltage balancing and individual DC voltage balancing algorithm. The results show that CPS-PWM technique results in a converter with excellent output voltage performance and perfect harmonic performance with fundamental switching frequency. It is concluded that CPS-PWM is the preferred modulation technique for for small and medium scale MMC with reduced number of submodules as the case with the experimental prototype developed in this article.

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