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DESIGN AND DEVELOPMENT OF MODULAR MULTILEVEL CONVERTER FOR SOLID STATE TRANSFORMER APPLICATION

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ABSTRACT

Unlike conventional line frequency transformer (LFT), solid state transformer (SST) is a power electronic device consisting of one or more converters that are based on semiconductor switches. However, the two-level and three-level voltage source converters (VSCs) used in SST lack scalability to higher voltage levels. This paper proposes a modular multilevel converter (MMC) based SST which allows the output voltage level to be varied without complexing the circuit. The proposed MMC based SST including the control method was validated in a detailed model of MMC with 20 SMs per arm in MATLAB® using Simulink® and PLECS® toolboxes. Experimental results are also presented on a scaled down laboratory prototype which validate the effectiveness of the proposed model. Simulation and experimental results show that multilevel voltage waveform can be conceived by adding more cells to the arms, thus allowing scalability to higher voltage and power levels.

Keywords: Modular multilevel converter (MMC); solid state transformer (SST); submodule (SM); capacitor voltage; circulating current.

1. INTRODUCTION

Solid state transformer (SST) is a power electronics based transformer that transforms 50 or 60Hz alternating current (AC) voltage to a high frequency one which is further stepped up/down by a high frequency transformer (HFT) with appreciable decrease in volume and weight, and finally, shaped back into the desired 50/60Hz voltage (Kadandani et al., 2019). It is one of the recent emerging technologies in smart grid (She and Huang, 2013) and power distribution system (She et al., 2013). Apart from voltage transformation, SST provides flexible methods for interfacing renewable energy sources with power grid with improved methods of controlling the routing of electricity and power flow, and safe operation of the grid. Other additional features and functions of SST include reduced size and weight, instantaneous voltage regulation, fault isolation, power factor correction, control of active and reactive power flow, fault current management on low-voltage and high voltage side, active power filtering of harmonic content on the input side, good voltage regulating capabilities, possibility of a direct current (DC) input or output, voltage dip/sag ride though capability (with enough energy storage) and smart grid integration (She and Huang, 2013).

SST con be configured as single-stage with no DC link, two-stage with a DC link on the secondary side, two-stage with a DC link on the primary side and three-stage with a DC link on both primary and secondary sides (Falcones et al., 2010). However, the three-stage SST is the most feasible configuration that allows enjoying all the benefits associated with SST.

It is the preferred choice for high power applications by designing each of the three conversion stages of the configuration using multilevel converter topologies (Ling et al., 2011; Roasto, et al., 2012). In this research, a three stage SST is considered. The configuration has the advantage of having DC link at both low and high voltage sides making it is easier to reject disturbances. Other advantages of this configuration include high flexibility, independent reactive power control, input voltage sag ride through capability, good output voltage and input current regulation, very simple modularity implementation, under and overvoltage protection, voltage sag compensation, renewable energy resources and energy storage integration as well as superior controllability (Falcones et al., 2010).

Figure 1 shows the block diagram of a three-stage SST with control method. The chosen configuration consists of three conversion stages, namely; a high-voltage AC-DC power converter that generates a high voltage DC bus, a high-frequency DC-DC converter that produces a regulated low voltage DC bus, and a DC-AC converter that produces a regulated low voltage AC bus (Viktor et al., 2011). Thus, the 50Hz AC voltage is transformed into a high frequency voltage followed by stepping down of the high frequency and finally shaping it back to the desired level at 50Hz (Huang, 2016). The input AC-DC converter is responsible for absorbing active power from the source (AC grid) and feed it to the next stage. The other task for this unit is the control of reactive power for grid services (Liserre et al., 2016). The DC-DC conversion block provides galvanic isolation between the high voltage side and the low voltage side. In this stage, the low frequency high voltage input AC signal of the SST is transformed into low voltage high frequency. This kind of converter is required to have high rated power, high current capability on the low voltage side, high voltage capability on the high voltage side, high frequency isolation and high efficiency. The output DC-DC converter is located on the low voltage side. As such, it has to supply the highest current among the three stages. It is the most exposed to the disturbances on the load side.

The two DC links allow for the AC power flow separation between the high voltage (HV) and low voltage (LV) grids. This feature enables controlling the two grids independently, with only the constraint of the active power link. The high voltage direct currents (HVDC) link works as a connection point between SSTs and can host new loads, like fast charging electric vehicle stations and distributed resources, large photovoltaic and wind power plants, and battery energy storage systems. It also enables DC Distribution system, HVDC applications and is ideal for connecting the remote offshore platforms and wind farms to the onshore grid. The low voltage direct current (LVDC) link offers the possibility to connect the DC loads directly to LVDC grid, avoiding an intermediate conversion stage at the user's site. It also supports integration of renewable energy sources, power quality related features such as power factor correction, reactive power compensation and active filtering, DC microgrid, smart grid interfacing DC sources, loads and storage units.

The control strategy include a direct-quadrature (DQ) synchronous frame controller on the AC-DC converter based on the method proposed by Kadandani et al., (2019) for regulating the HVDC link voltage to its reference value and for the control of reactive power for grid services. In the DC-DC converter, a phase shift control is employed for achieving a smooth power transfer from the primary to the secondary converter and at the same time regulating the LVDC link voltage to its reference value. The DC-AC converter control is based on the method proposed by Hagiwara and Akagi, (2010) and it consists of two control algorithms, namely; individual DC capacitor voltage balancing control for regulating the individual voltages in each sub-module (SM) to their reference value, arm balancing control for suppressing any voltage and averaging control for regulating the average capacitor voltage to the reference value.

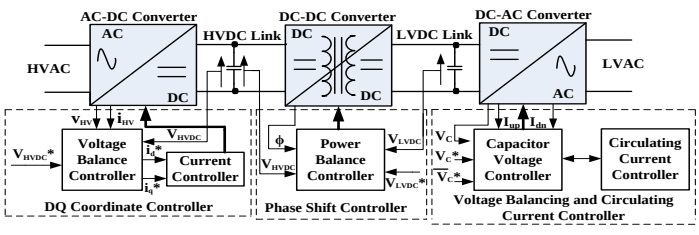

Figure 1: Block Diagram of SST with Control Method

SST have been considered as a substitute of LFT with improved functionalities. She, Huang & Burgos (2013) compared the performance of LFT with modern SST in terms of active power transfer, reactive power compensation, and voltage conversion functionality in WECS. Simulation results shows that the SST approach provides better voltage regulation and can fulfil the tasks of active power transfer, reactive power compensation and voltage-step better than LFT.

She et al. (2013) investigated how SST can perform the integrated functions of active power transfer, reactive power compensation, and voltage conversion in WECS. The result shows that SST can effectively suppress the voltage fluctuations caused by the transient nature of wind energy without additional reactive power compensator and, as such, may enable the large penetration of WF into the power grid.

Wang & Liang (2015) investigated the voltage ride through capability of SST in grid-connected system. The results show that during voltage sag caused by grid faults, energy storage devices connected to the SST discharges to sustain the LVDC bus voltage, enhancing the system low voltage ride through (LVRT) capability

Gao et al. (2017) investigates a medium-voltage SST based WECS with integrated active power management and reactive power compensation functions. Scenarios considered include the grid-connected mode, the islanding mode, and the mode transitions. Simulation results are provided to verify the effectiveness of the proposed strategy. The proposed system is found worthy of addressing the high transmission losses and bulky LFT issues associated with the conventional Static synchronous compensator (STATCOM) based WECS. It can be seen from the literature review that SST is an emerging technology that can replace the bulky LFT in voltage transformation with additional ancillary services to the grid such as reactive power compensation / harmonic filtering, disturbance and fault isolation and many more. SST is also being considered in grid integration of renewable energy sources such as wind, where it can provide a direct substitute for STATCOM, its coupling transformer, the bulky step-up LFT and active power filter (APF). In fact, SST can be used for power quality improvement in grid connected wind farms faster than STATCOM. In traction and other locomotives, SST is also being considered as a direct substitute of LFT for decreased space and volume.

2. AN OVERVIEW OF MODULAR MULTILEVEL CONVERTER

Modular multilevel converter (MMC) was proposed by Lesnicar and Marquardt (2003) and has become the preferred choice for HVDC transmission system (Saeedifard and Iravani, 2010), medium voltage drives (Antonopoulos et al., 2014), flexible alternating current transmission system (FACTS) (Pirouz and Bina, 2010) and in SST system (Andresen et al., 2017). Unlike two-level and three-level voltage source converters (VSCs), the output voltage level of MMC can be varied without complexing the circuit. Multilevel voltage waveform can be conceived by adding more cells to the arms, thus allowing scalability to higher voltage and power levels. Other advantages of MMC over two-level and three-level VSCs include; distributed location of capacitive energy storage (Perez et al., 2015), output voltage waveform with very low ripple content (Li et al., 2015), lower switching losses and higher efficiency (Ilves et al., 2012), simple capacitor voltage balancing control and reduced EMI noise (Goetz et al., 2015).

Figure 2 shows the circuit topology of three phase MMC for the study case. Each phase has two arms; - upper and lower. Each arm has N number of SMs and an arm inductor. The SM used is of half bridge SM (HBSM) configuration because of its simplicity in terms of component count.

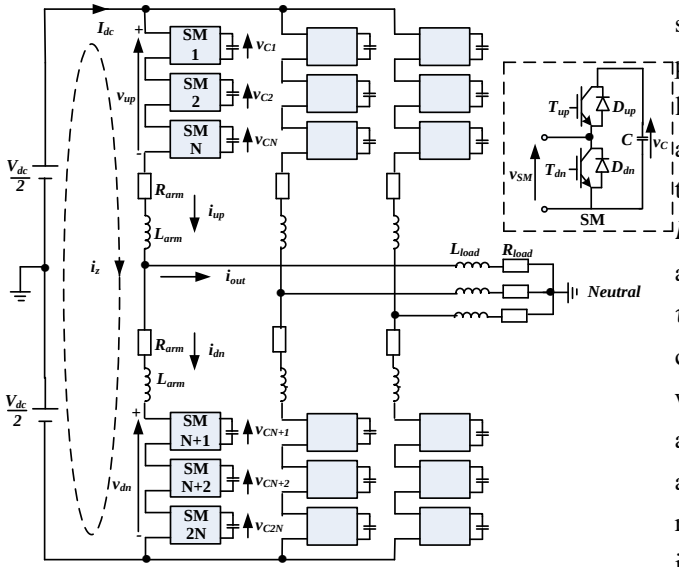

Figure 2: Circuit Topology of the MMC for the Study Case

Each of the HBSM consists of two controlled semiconductor switches with associated anti-parallel diodes, and a DC capacitor for energy storage. The arm inductance is used to limit the amplitude of the circulating current through the arm and possible fault current. It also allows small mismatch in the arm voltages. V_{dc} is the input DC voltage, L_{arm} and R_{arm}, are the arm inductance and its resistance, i_{up} and i_{dn} are the currents through the upper and lower arm respectively, v_{up} and v_{dn} are the respective arm voltages, i_z is the circulating current that flows within the arms of the converter without appearing at its output, L_{load} and R_{load} represents an RL load, i_{ac} and v_{ac} are the output AC current and voltage respectively, i_{SM} and v_{SM} are SM current and voltage respectively, C is the SM capacitor and v_C is the SM capacitor voltage, T_{up} and D_{dn} are the upper insulated bipolar junction transistor (IGBT) and diode in the SM while T_{dn} and D_{dn} are the lower IGBT and diode in the SM.

3. CONTROL METHOD

3.1. Average DC Voltage Control

The average DC voltage control is meant to force the average capacitor voltage in upper arm $\overline{v_{C\_up}}$ to follow its reference value $v^*_{avg\_up}$ and also to force the average capacitor voltage in lower arm $\overline{v_{C\_dn}}$ to follow its reference value $v^*_{avg\_dn}$ (Hagiwara and Akagi, 2010).

$$\overline{v_{C\_up}} = \frac{1}{N}\sum_{k=1}^{N} v_{Ck} \quad (1)$$

$$\overline{v_{C\_dn}} = \frac{1}{N}\sum_{k=N+1}^{2N} v_{Ck} \quad (2)$$

Figure 3 shows block diagram of average DC capacitor voltage balancing control strategy.

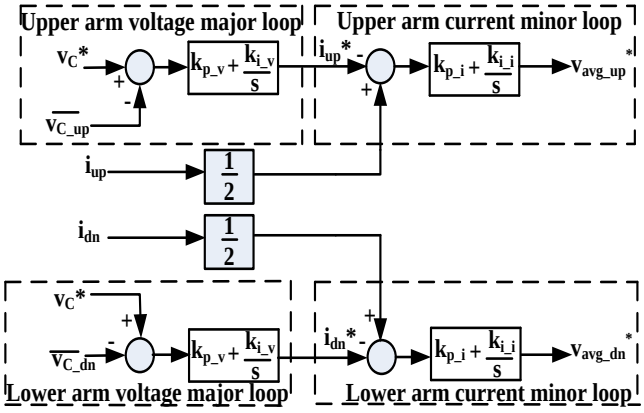

Figure 3: Block Diagram of Average DC Voltage Control

The current reference of the upper arm, i^*_{up} can be represented as:

$$i^*_{up} = k_{p\_v}\left(v^*_C - \overline{v_{C\_up}}\right) + k_{i\_v}\int\left(v^*_C - \overline{v_{C\_up}}\right)dt \quad (3)$$

where k_{p_v} and k_{i_v} are the respective proportional and integral gain in voltage major loop.

Following the same passion, the current reference of the lower arm, i^*_{dn} can be represented as:

$$i_{dn}^{*} = k_{p\_v}\left(v_C^{*} - \overline{v_{C\_dn}}\right) + k_{i\_v}\int\left(v_C^{*} - \overline{v_{C\_dn}}\right)dt \qquad (4)$$

The voltage command from the averaging control for the upper arm, $v_{avg\_up}^{*}$ can now be expressed as:

$$v_{avg\_up}^{*} = k_{p\_i}\left(i_{up} - i_{up}^{*}\right) + k_{i\_i}\int\left(i_{up} - i_{up}^{*}\right)dt \qquad (5)$$

where k_{p_i} and k_{i_i} are the respective proportional and integral gain in current minor loop.

Following the same passion, the voltage command from the averaging control for the lower arm, $v_{avg\_dn}^{*}$ can be expressed as:

$$v_{avg\_dn}^{*} = k_{p\_i}(i_{dn} - i_{dn}^{*}) + k_{i\_i}\int(i_{dn} - i_{dn}^{*})dt \qquad (6)$$

As can be seen in figure 3, the action of the controller depends on the value of $\overline{v_{C\_up}}$ and i_{up}. As it can be seen from (3) that, when $v_C^{*} \geq \overline{v_{C\_up}}$, the controller increases the value of i_{up}^{*} so that i_{up} follows the value of i_{up}^{*}. Accordingly, $\overline{v_{C\_up}}$ follows v_C^{*} without any impact on i_{ac}. The same scenario applies to the lower arm.

3.2. Individual DC Voltage Control

The individual DC voltage control is to ensure that each individual capacitor voltage V_{ck} $(k: 1\sim 2N)$ follows its reference value yielding v_{bal}^{*} as the resulting voltage command. However, this control is based on either i_{up} or i_{dn}, as such, the polarity of v_{bal}^{*} has to change according to that of the arm current.

Figure 4 shows the block diagram of the individual DC capacitor voltage balancing control strategy.

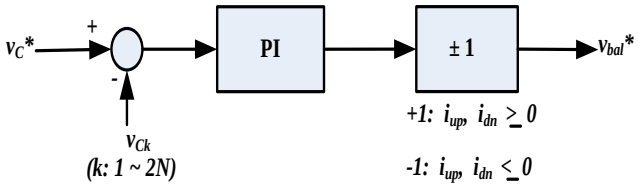

Figure 4: Block Diagram of Individual DC Voltage Control

As can be seen in figure 4, the action of this controller is such that:

When $i_{up}, i_{dn} \geq 0$, v_{bal}^{*} is expressed as:

$$v_{bal}^{*} = k_p(v_C^{*} - v_{Ck}) \qquad (7)$$

Conversely, when $i_{up}, i_{dn} \leq 0$, v_{bal}^{*} is expressed as:

$$v_{bal}^{*} = -k_p(v_C^{*} - v_{Ck}) \qquad (8)$$

where k_p is the proportional gain of the P controller in the individual DC capacitor voltage balancing control.

4. DESIGN OF PASSIVE COMPONENTS

4.1. Design of Submodule Capacitor

The SM capacitor serves as DC energy storage of the SM. It is an important part of MMC and plays significant role in determining the capacity and cost implication of the converter. Proper sizing of SM capacitor will limit voltage and current ripples in the converter. Tang et al., (2014) proposed an analytical model for designing SM capacitor is developed based on four major criteria; maximum capacitor voltage, voltage ripple, current ripple and SM voltage capability. The idea behind considering the maximum capacitor voltage is to prevent rapid ageing. Accordingly, considering the amount of voltage excess, $V_{\max p.u}$ the SM capacitor, C should be sized based on the following (Tang et al., 2014):

$$C \geq \frac{\sqrt{2}NI_{ac}}{\omega V_{\max p.u} V_{dc}} f_{max}(m,\varphi) \qquad (9)$$

where N is the number of SMs in an arm, I_{ac} is the magnitude of the rms value of the AC side current, ω is the fundamental angular frequency , V_{dc} is the rated DC-link voltage, m is the modulation index, φ is the power factor angle and $f_{max}(m,\varphi)$ is the voltage excess function.

On the other hand, when the value of permitted ripple voltage, $V_{\text{ripple } p.u}$ is considered in the design, then the SM capacitor should be sized based on the following (Tang et al., 2014):

$$C \geq \frac{\sqrt{2}NI_{ac}}{\omega V_{\text{ripple } p.u} V_{dc}} f_{ripple}(m, \varphi) \quad (10)$$

4.2. Design of Arm Inductor

The main functions of arm inductance are to suppress the second order harmonic component of circulating current through the arm and to limit fault current in the event of DC short circuit fault. Accordingly, the selection of a suitable arm inductance is primarily determined by the requirement on the low frequency circulating current suppression and limiting the short circuit fault current (Dorn et al., 2007). Based on this, Tu et al., (2010) developed analytical relationship relating the arm inductance with the double line frequency circulating current on one hand and with the DC fault current rise rate on the other hand.

Equation (11) gives the relationship between the arm inductance and peak value of the circulating current (Tu et al., 2010).

$$L_{arm} = \frac{1}{8\omega^2 C V_C}\left(\frac{P_s}{3I_{2f}} + V_{dc}\right) \quad (11)$$

where ω is the fundamental angular frequency, C is the capacitor of the SM, V_C is the DC component of the capacitor voltage, P_s is the apparent power, I_{2f} is the peak value of the AC component of the circulating current i_{2f} and V_{dc} is the rated DC bus voltage.

Equation (12) on the other hand relates the arm inductance with the DC fault current rise rate σ, (Tu et al., 2010).

$$L_{arm} = \frac{V_{dc}}{2\sigma} \quad (12)$$

5. SIMULATION RESULTS AND DISCUSSION

The simulation of the converter and its control strategy was implemented in MATLAB® using Simulink® and PLECS® toolboxes based on system parameters shown in table 1. The results are presented in figure 5 through 7.

Figure 5 shows the current waveform at the output, upper arm and lower arm of the converter. As can be seen in the figure, the arm currents consist of double frequency component due to the AC component of the circulating current while the output waveform is seen to be of smooth sinusoidal waveform. Circulating current is an inherent feature of MMC. It is as a result of the variation in the instantaneous voltages among the three phases of the converter that arise from the voltage variation in the DC capacitor voltages. Incidentally, it does not affect the outer dynamics of the converter, as such the output AC current of the converter is of smooth sinusoidal waveform as shown in figure 5. Thus, the power quality of the system is guaranteed.

Figure 6 shows the output voltage and multilevel arm voltages. During operation, an SM toggles between on-state and off-state. During the on-state, the terminal voltage of the SM is zero, whereas during the off-state, the voltage assumes the value of its module capacitor, v_C (DC energy storage of the SM). The switching sequence of upper and lower arms are complementary. The output of the series connected SMs are combined to generate appropriate multilevel arm voltage, v_{up} or v_{low}. The DC capacitor of an SM can either contribute to the output voltage or be bypassed, hence, v_{up} and v_{low} collaborate to yield the desired v_{ac}. The sum of v_{up} and v_{low} is equal to the value of V_{dc}. This implies that the AC and DC sides of the converter can be independently controlled. During operation, the output AC voltage waveform, v_{ac} is synthesised by either subtracting the sum of SM voltages in the upper arm, v_{up} from the positive terminal of the DC link or by adding the sum of SM voltages in the lower arm, v_{low} from the negative terminal of the DC link. In this passion, v_{ac} will assume its maximum value when all the upper arm SMs are deactivated and minimum value when all the lower arm SMs are activated. As such, the control strategy of the two arms has to be complementary and their voltages has to match. In other words, deactivated SMs in the upper arm has to have corresponding number of activated SMs in the lower arm.

Figure 7 shows the SM capacitor voltages. It can be seen that the average DC voltage control was able to force the average DC capacitor voltage of each arm to follow its reference value and the individual DC voltage control was also able to force the SM capacitor voltages of individual SMs to follow their reference value. The effectiveness of the two cascaded capacitor voltage balancing control loops can be judged from figure 7 where it can be seen that the capacitor voltage variation is regulated within 5V peak to peak.

Table 1: MMC System Parameters for Simulation

Parameter	Value
Input DC Voltage	20kV
Output AC Voltage Reference	10kV
Arm Inductance	10mH
Number of Sub-Modules Per Arm	20
Sub-Module Capacitance	10mF
Sub-Module Capacitor Voltage Reference	1kV
Carrier Frequency	2kHz

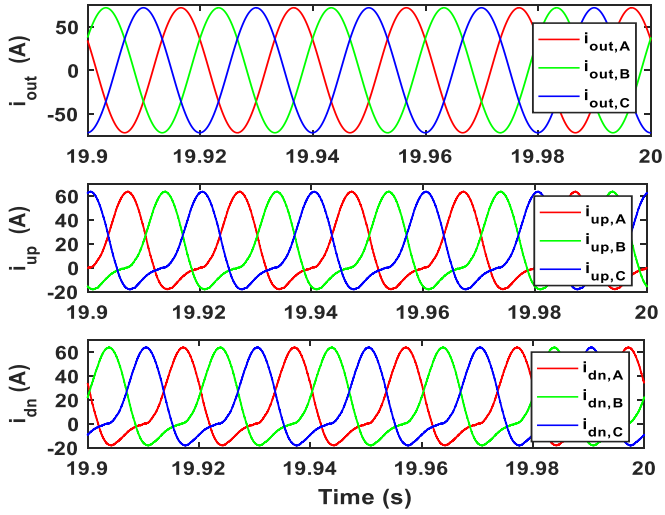

Figure 5: Output Current, Upper Arm Current and Lower Arm Current of the Simulated MMC

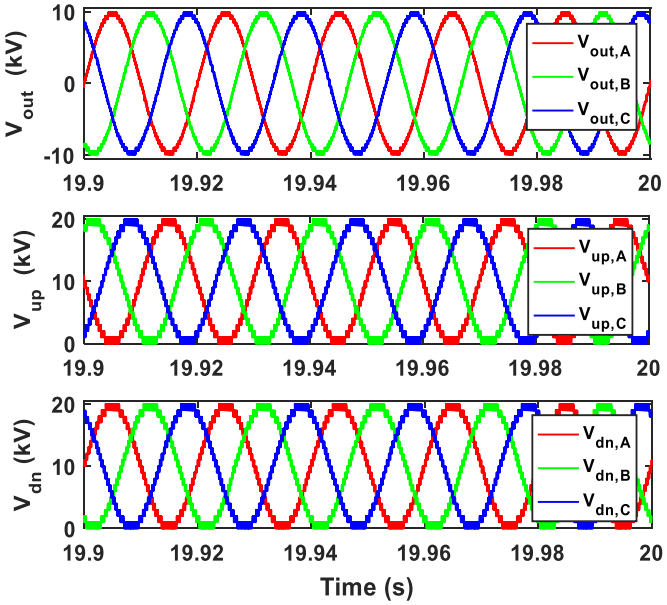

Fig. 6: Output Voltage, Upper Arm Voltage and Lower Arm Voltage of the Simulated MMC

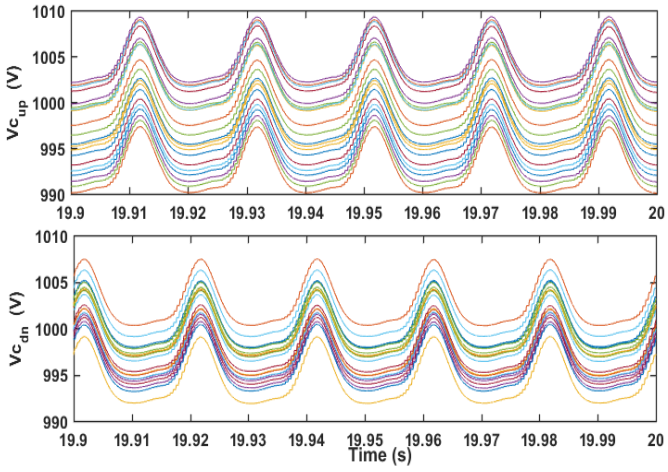

Figure 7: Sub-module Capacitor Voltages of one Phase of the Simulated MMC

6. EXPERIMENTAL VALIDATION

It is a well-known fact that modular multilevel converters are intended for high voltage high power applications as demonstrated in the simulation for a close-to-reality system. However, experimental implementation of such system requires huge resources in terms of software and hardware in addition

to safety issues that have to be assessed in the laboratory. Therefore, a scaled-down version can be used as a proof of concept for validating the proposed control method. For the validation of the simulation results, an experimental desk has been developed on a scaled down laboratory prototype MMC based on system parameters shown in table 2. Figure 8 shows the experimental test rig while figure 9 shows the overall connection and communication structure for the control of the experimental MMC prototype.

The DSP used in the control is TMS320F28377D Dual-Core Delfino™ Microcontroller board (Datasheet) while code composer studio (CCS) ("Code Composer Studio,") was used as the coding environment. A MATLAB graphical user interface (GUI) is used with the control board and are linked via USB cable. It is meant to set up the GUI appearance and operate continuous communications with the target hardware (TMS320F28377D control board).

The results of the experimental set-up are presented in figure 10 through 13. Figure 10 present the output current, upper arm and lower arm current of the converter while figure 11 shows the voltage waveforms at the output, upper arm and lower arm of the converter. Figure 11 depicts the SM capacitor voltages in the upper and lower of the converter. All the experimental results show similar agreement with the simulation results, thus confirming voltage and power level scalability of MMC required for SST applications.

Table 2: Parameters of the MMC Prototype

Parameter	Value
Number of Submodule Per Arm	3
Submodule Capacitance	2.2mF
Arm Inductance	1mH
Load Resistor	33Ω
Load Inductor	1mH
DC Link Voltage	100V
Carrier Frequency	4kHz
Modulation Index	0.9

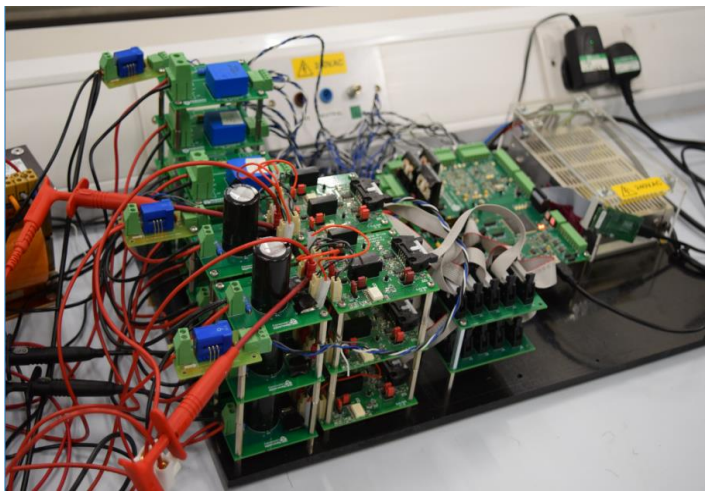

Figure 8: Experimental Test Rig

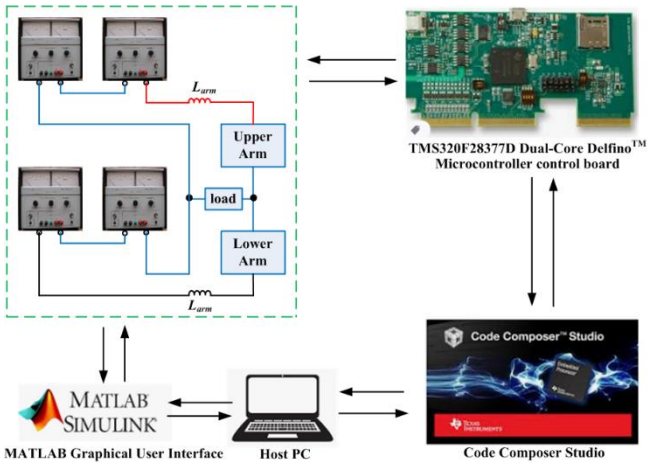

Figure 9: Connection and Communication Structure for the Control of the Experimental MMC Prototype

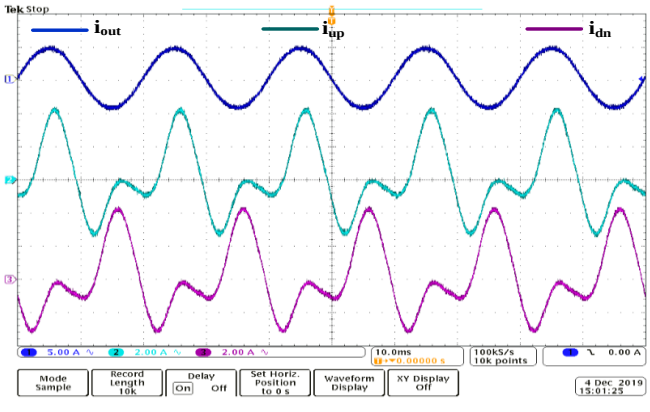

Figure 10: Output Current, Upper Arm Current and Lower Arm Current of the Experimental MMC

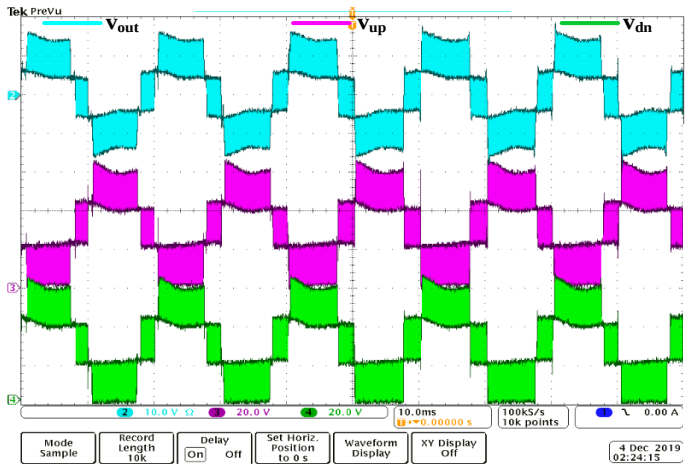

Fig. 11: Output Voltage, Upper Arm Voltage and Lower Arm Voltage of the Experimental MMC

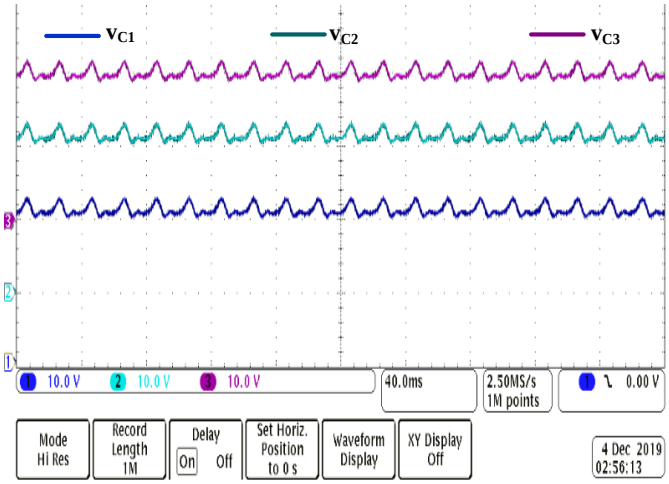

Figure 12: Sub-module Capacitor Voltages in Upper Arm of the Experimental MMC

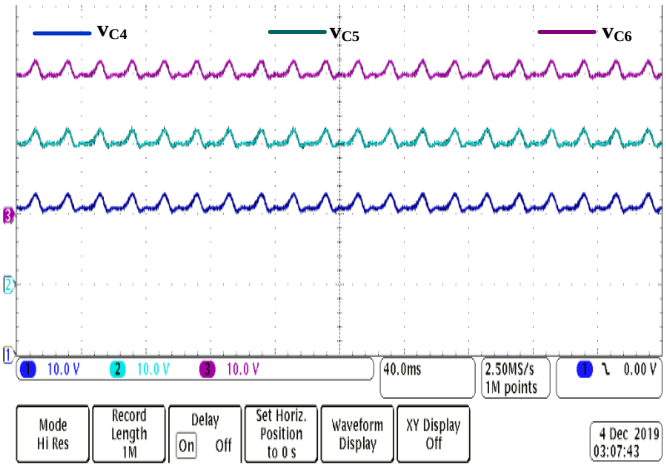

Figure 13: Sub-module Capacitor Voltages in Lower Arm of the Experimental MMC

7. CONCLUSION

The paper has presented simulation and hardware implementation of modular multilevel converter for solid state transformer applications. Design details and simulation of a close to reality 1kVA MMC is presented based on distributed method of capacitor voltage balancing algorithm. The control strategy is based on regulating average and individual SM capacitor voltages to their respective reference values. An experimental implementation of a scaled down prototype converter was also presented for validating the Simulink model. The laboratory prototype is a single phase MMC with three SMs per arm. The control algorithm was implemented in code composer studio using TMS320F28377D microcontroller and MATLAB GUI. Results from the Simulink model and experimental prototype shows that MMC allows scalability to higher voltage and power levels by simply adding more cells to the converter arms. As such, when used in SST, a higher rating scalable device can be conceived without complexing the circuit.

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