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HARDWARE IMPLEMENTATION OF MODULAR MULTILEVEL CONVERTER PROTOTYPE FOR HVDC TRANSMISSION SYSTEM

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ABSTRACT

Due to its modularity, scalability and low power losses, the modular multilevel converter (MMC) is being considered as the most promising converter for high voltage direct current (HVDC) transmission system against conventional two-level and three-level voltage source converters (VSC). This paper presents hardware implementation of MMC laboratory prototype for HVDC transmission system. The hardware prototype is made of MMC with four submodules (SM) per arm while the digital signal processor (DSP) used in the programming is Texas Instrument (TI) TMS320F28377D Dual-Core Delfino™ Microcontroller board with the code written in code composer studio (CCS). The results of the experiment show that the MMC prototype exhibits improved quality of the AC side current with reduced harmonic distortion, improved quality of the output staircase voltage of nearly sinusoidal waveform, high efficiency, reduced electromagnetic interference (EMI) noise, and low switching frequency which are the major requirement of HVDC system that could not be achieved with the conventional two-level and three-level VSCs.

Keywords: High voltage direct current (HVDC); modular multilevel converter (MMC); voltage source converter (VSC); current source converter (CSC), line commutated converter (LCC).

1. INTRODUCTION

High voltage direct current (HVDC) system is the preferred means of transmitting bulk electric power over long distance with reduced losses (Teng & Li, 2020). It is widely used for long-distance power transmission and interconnecting different units of power grid or with distributed generations such as wind farms where the turbines are installed far away from the shore (Khazaei, Idowu, Asrari, Shafaye, & Piyasinghe, 2020) as demonstrated in (Beza & Bongiorno, 2019; Jiao & Nian, 2020; Zhang, Klabunde, & Wolter, 2020). The system is made up of converter station where the AC system is first converted into DC, transmitted through power transmission cable and finally converted back into AC. The HVDC transmission system allows simpler design of towers, smaller footprint and reduced costs of conductors and installation. Typically, HVDC transmission system uses ground as a return path; as such, tower requirement is simplified which in turn reduces the system cost (Abouelatta et al., 2020).

HVDC can be configured in one of three forms; monopolar, bipolar and back-to-back configuration. The monopolar configuration is a system in which two converter stations are interconnected together via a single line with metallic conductor, ground or sea as the return path. In this arrangement, both DC polarities can be operated. In bipolar configuration however, two conductors are operated at opposite polarities giving two independent DC circuits; each at half capacity rating. On the contrary, the back-to-back configuration involves connecting the DC sides of two converter stations directly with no DC transmission line. Nowadays, the most common HVDC system is the bipolar configuration.

The HVDC configuration is categorised into two distinct technologies; line commutated converters (LCC) based HVDC and voltage source converters (VSC) based HVDC. The former is usually realised using current source converters as demonstrated in (Luan et al., 2019; H. Wu, Liu, Wang, Song, & Wu, 2019) and the later using two-level and three-level converters as demonstrated in (Elgeziry et al., 2019; W. Wu et al., 2018) as well as using modular multilevel converter (MMC) as in (Han et al., 2018; Hao, Li, Gao, & Zhang, 2019; Zhu, Lin, Dinavahi, & Liang, 2020).

LCC-HVDC transmission system is typically meant for high capacity power transmission in the range of Giga-Watts with a transmission voltage of ±1,1000kV for a distance of up to 3,00km (Schönleber, Oudalov, Krontiris, & Lundberg, 2020). LCCs were manufactured with electronic switches to be turned on. Before 1970s, LCCs were manufactured with mercury arc valve while those manufactured after 1970s were made with thyristor valve (Hannan et al., 2018).

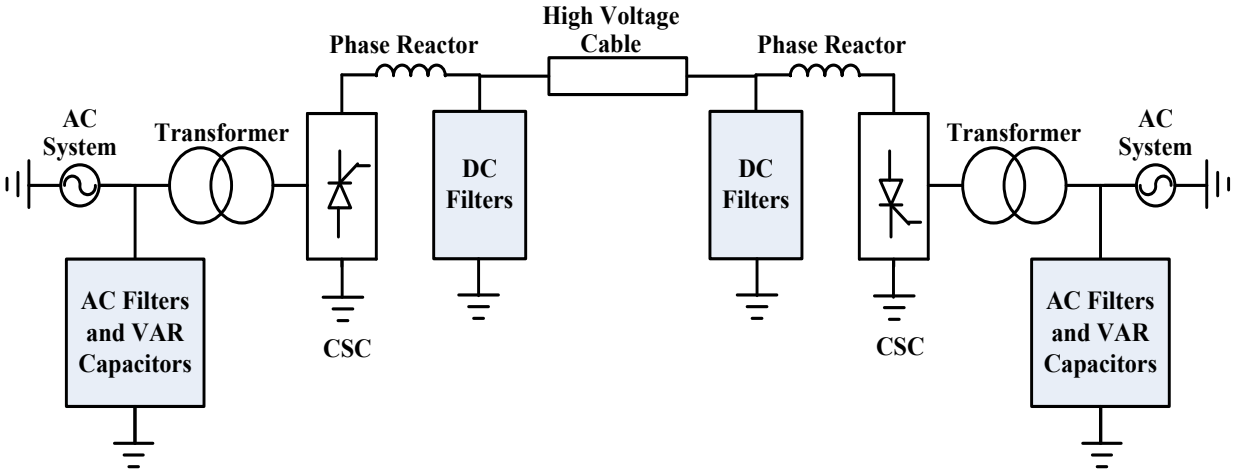

Figure 1: CSC-HVDC Configuration

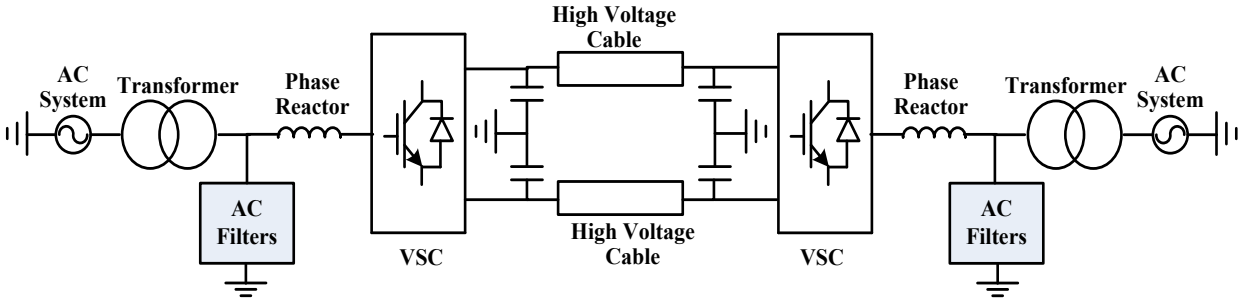

Figure 2: VSC-HVDC Configuration

Modern LCC-HVDC uses thyristors based line-commutated converters with transformers being used to connect the converter stations with the AC system. The system is also equipped with filters for suppressing the harmonics in both AC and DC sides. The power level is controlled by changing the switching pulses/firing angles of the thyristors based line-commutated converters. Figure 1 shows a single line diagram of CSC-HVDC configuration. It can be seen that reactive power compensation is achieved with the help of Var capacitors while inductors are used in the DC sides to suppress voltage ripple. The main advantage of CSC-HVDC system is its capability to control current in the DC side of the system under fault conditions (Elgamasy, Talaab, Kawady, Izzularab, & Elkalashy, 2020). The major drawbacks of CSC-HVDC system are the need for Var compensation due to consumption of reactive power, the necessity for synchronous voltage source for commutation, the necessity of polarity change for reverse power flow, the need for bulky filters and the requirement of an AC grid for proper operation (Sánchez-Sánchez, Prieto-Araujo, Junyent-Ferré, & Gomis-Bellmunt, 2018).

In VSC-HVDC transmission system however, two converter stations are used to interconnect two independent AC networks with two DC conductors of opposite polarities. In this system, the VSC serves as controllable voltage source capable of providing AC voltage of desired magnitude and phase for active and reactive power exchange with the AC system. It uses self-commutated valves of insulated-gate bipolar transistor (IGBT). The power transmission capacity of VSC-HVDC is in the range of Mega-Watts with a transmission voltage of ±525kV (Schönleber et al., 2020). Figure 2 shows a single line diagram of VSC-HVDC configuration. Typically IGBTs are used as the semiconductor switches in

this type of configuration. As can be seen in Figure 2, the main components of a typical VSC-HVDC system are AC-side transformer, phase reactor, AC-side filters, DC-side capacitor and DC line. The functions of the AC-side transformer is to provide galvanic isolation between the converter station and the main AC system, prevent the possible propagation of harmonics to the AC system and to ensure proper connection of the variable voltage AC system with the converter. The purpose of the phase reactor is to ensure smooth and efficient active and reactive power transfer between the converter station and the remaining parts of the AC system. It also filter the higher harmonic components from the output current of the converter. The AC-side filters are usually passive filters employed in the VSC-HVDC system to filter out the harmonic component of the output voltage. The DC-side capacitor on the other hand is required to suppress the voltage ripple on the DC side of the HVDC system. They also serve as energy storage allowing the converter to store or absorb energy. The DC-line are the transmission link between the VSC-HVDC stations. VSC-HVDC system therefore enhance the stability of the surrounding AC grid due to its fast and independent control of active and reactive power (Gonzalez-Torres, Damn, Costan, Benchaib, & Lamnabhi-Lagarrigue, 2020).

Initial attempts of VSC-HVDC systems are based on two-level converters and three-level neutral point clamped (NPC) converters. The former can switch between two levels only; $\frac{V_{dc}}{2}$ and$\frac{-V_{dc}}{2}$ yielding voltage waveform with high harmonic content making filtering a major requirement. The latter can switch to three levels; $\frac{V_{dc}}{2}$, 0 and $\frac{-V_{dc}}{2}$ yielding voltage waveform with lower harmonic content that still need to be filtered. Both two-level and three-level VSCs allows independent reactive power control at either terminal, provide efficient black starting and fault ride-through capability, offers possibility of connecting weak and passive grids, eliminate the need of special converter transformers, allows fast active power reversal, it does not require commutating source voltage (L. Wang, Yang, Lu, & Prokhorov, 2017; Ye, Lu, Xie, & Qiao, 2018). However, the major drawbacks of two-level and three-level VSC-HVDC configuration are the possibility of high short circuit current from the energy stored in the DC bus which can lead to damage and the possibility of electromagnetic interference in the arm current can add extra stress to the semiconductor devices.

The emergence of modular multilevel converter (MMC) and its consideration for HVDC system has provide solutions to the problems of the conventional two-level and three-level VSC-HVDC configurations. The MMC technology has the advantage of modularity, and scalability to different voltage and power levels, improved power quality, fault blocking capability, reduced voltage ratings, inherent fault-tolerance capability and high efficiency, less semiconductor device stress, reduced electromagnetic interference (EMI) noise, and low switching frequency (Ansari, Liu, & Khan, 2020; Jamshidifar & Jovcic, 2015). The only disadvantage of MMC is the circulating current arising from inner voltage differences among each phase unit of the converter. It is caused by DC capacitor voltage variations leading to variations in the instantaneous voltages among the three phases of the converter (Kadandani, Dahidah, & Ethni, 2021b). It usually manifests itself in the form of second order harmonics on the arm currents of the converter (Kadandani, Dahidah, & Ethni, 2021a). However, circulating current can be controlled to enable proper operation of the converter. Circulating current control (CCC) methods in MMC have been addressed in (Chen, Liu, Song, & Ouyang, 2020; Pérez-Basante et al., 2020; Tanta et al., 2020). MMC uses standard components such as insulated gate bipolar junction transistor (IGBT) to achieve scalability to different voltage and power levels (Harnefors, Antonopoulos, Norrga, Angquist, & Nee, 2013).

Nevertheless, VSCs family enable better transmission efficiency, independent and flexible power control, reactive power compensation, and unlimited terminal configurations (Y. Wang et al., 2019), as such, VSC-HVDC is the preferred choice for efficient and reliable bulk power transmission with improved power quality and controllability (Diez, Costabeber, Tardelli, Trainer, & Clare, 2020).

The remaining part of this paper is organised as follows; section 2 presents MMC-HVDC system configuration while section 3 presents the control technique. Experimental demonstration is presented in section 4. Results and discussion are presented in section 5. Finally, section 6 concludes the paper.

2. MMC-HVDC SYSTEM CONFIGURATION

MMC was first introduced by Marquardt and Lesnicar in 2002 (Marquardt, 2002) while the details of the converter, its control strategy and modulation techniques were further elaborated in 2003 (Lesnicar & R.Marquardt, 2003). Unlike two-level and three-level converters, MMC has output voltage with lower harmonic content, and achieve high voltage and large capacity (Ahmed, Angquist, & mahmood, 2015; Hu, Xu, Lin, & Zeng, 2017). MMC has now emerged as the most promising technology for HVDC transmission system. A single-line diagram of MMC-HVDC configuration is shown in Figure 3. The major advantages of this configuration include freedom of adding both the rated voltage and

power of the system, elimination of high DC link capacitor because each submodule of the configuration has its own capacitor and possibility of eliminating AC filters because of the inherent harmonic reduction offered by the staircase multilevel voltage waveform.

The main advantages of MMC-HVDC configuration include outstanding output performance, scalability to different voltage and power rating by increasing the number of SMs, robustness by using redundant SMs, improved quality of the AC side current with reduced harmonic distortion due to multilevel waveform, elimination of filters and HVDC link capacitor banks resulting in smaller footprint, and harmonic characteristics (Adam et al., 2017; Shi, Filizadeh, & Jacobson, 2018).

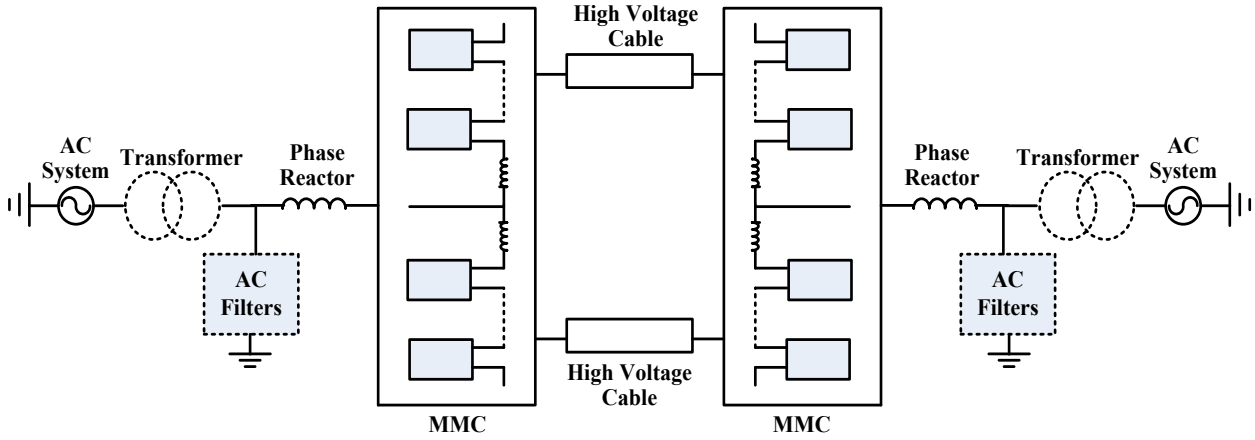

Figure 3: MMC-HVDC Configuration

3. CONTROL TECHNIQUE

3.1. Converter Control

The converter control was implemented in Texas Instrument TMSF28377D Dual-Core Delfino™ microcontroller board with code composer studio. It was built in two cascaded control loops, namely; average DC capacitor voltage balancing control and individual DC capacitor voltage balancing control.

The average DC capacitor voltage balancing control is meant to force the average DC capacitor voltage to follow its reference value. This control algorithm is based on comparing the average capacitor voltage in upper arm, $\overline{v_{C\_up}}$ with its reference value, v_C^* and also comparing the average capacitor voltage in lower arm, $\overline{v_{C\_low}}$ with its reference value, v_C^*. Based on this, a controller is designed that will yield the required reference averaging voltage command in the upper arm, $v_{avg\_up}^*$ and that of the lower arm of the converter, $v_{avg\_low}^*$. The resulting reference averaging voltage commands, $v_{avg\_up}^*$ and $v_{avg\_up}^*$ were used as components in generating the reference modulating signal for sending appropriate switching signals to the converter semiconductor switches. Figure 4 shows the block diagram of the converter control based on average DC voltage balancing.

The individual DC capacitor voltage balancing control whose purpose is to force the DC capacitor voltages of individual SMs to follow the reference value. This control algorithm is based on comparing each individual capacitor voltage, v_{Ck} (k: 1~$2N$; N being the number of SMs per arm) with the reference value, v_C^* and designing a controller that

will yield a reference balancing voltage command, v_{bal}^{*} depending on the polarity of the current in the upper arm, i_{up} or that of the lower arm, i_{low}. The resulting reference balancing voltage command, v_{bal}^{*} is then used as a component in generating the reference modulating signal for sending appropriate switching signals to the converter semiconductor switches.

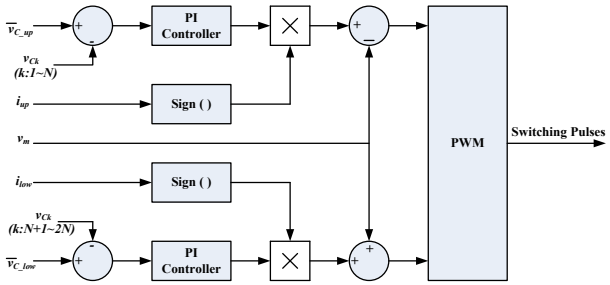

Figure 4: Block Diagram of the Converter Control

3.2. Code Composer Studio

The code was written in code composer studio (CCS). A MATLAB graphical user interphase (GUI) is used with the control board and are linked via USB cable. Digital signal processor (DSP) TMS320F28377D control board from Texas Instrument (Datasheet) is used in the experiment. The code was written in such a way that the TMS320F28377D peripheral initialization is done by one of the 32-bit central processing units (CPU1) while the converter control is mainly in the control law accelerator of the central processing unit (CPU1.CLA). The MATLAB GUI for control/monitoring of target is hosted on a laptop which communicates via serial commination interphase (SCI) register.

3.3. Control Board

As shown in Figure 5, the TMS320F28377D control board is a Single-Precision Floating-Point Unit (FPU) controller that has two TMS320C28x 32-bit central processing units (CPUs) each with 200 MHz processing capability. Each of the two CPUs has an associated Control Law Accelerator (CLA) with the same clock frequency as the CPU. The CLA is also a 32-bit, floating-point processing unit. The chip therefore has four processing units of computational capability. Each CPU within the TMS320F28377D also contains another two computational accelerators in the Trigonometric Maths Unit (TMU) and the Viterbi Complex Maths Unit (VCU). These units speed up various numerical calculations. The speed enhancements provided by these accelerators are invoked automatically by the C compiler and so do not require any consideration when writing code.

Figure 5: TMS320F28377D ControlCARD (Datasheet)

3.4. Graphical User Interphase (GUI)

The MATLAB GUI developed in the experiment contains a number of widgets (e.g. pushbutton, popup menu, text box, axis, and slider). Figure 6 shows a schematic appearance of the GUI. The 3 identical graphical axes on the left are used to display data or some selected control parameters. There are also a number of pushbutton. A pushbutton 'CLR' (yellow) is used to remove the displayed data from the associated axis. The 'PWM ON' (green) pushbutton is used to activate the target PWM. The 'PWM OFF' (red) pushbutton deactivates the target PWM. The 'STORE' (yellow) pushbutton starts the target data store process which self terminates when the data stores are full. The 'PLOT' (blue) pushbutton plots the data specified by the popup menu selection. The 'SKIP' pushbutton determines the effective sampling rate of the data store process. The number selected by 'SKIP' determines the number of interrupt service routines (ISR). The 'TRIP' indicator turns red when a PWM trip event occurs. There are also 2 columns of data boxes that are used to display numerical

data whilst the target is running. The data box ('Input 1' and 'Input 2') which can be used to enter numerical values which are sent to the target. The 4 sliders are used to send data to the target. The 'EXIT' GUI' (blue) button in the bottom right corner of the GUI is used to exit from GUI.

Figure 6: MATLAB Graphical User Interphase

3.5. Modulation Voltage Synthesis

The MMC control loops need to be linked to the *modulation voltage synthesis* for providing appropriate gate signals for the switches in the SMs. The main purpose of the modulation is to synthesize the AC waveform by activating SMs. Two modulator blocks (one for each arm of the converter) were developed and they work independently. Each modulator works in hand with voltage balancing controller in selecting and activating an SM. The output of the modulation in any arm is a multilevel pulse waveform. Carrier phase shifted pulse width modulation (CPS-PWM) technique that employs multiple carriers to control the semiconductor switches of the converter is used. The technique is good for converters with high number of levels as in the case of MMC in HVDC system. The CPS-PWM technique involved assigning one carrier for each cell to be modulated. The N carriers have the same frequency but are phase shifted by $360^{o}/N$ in order to generate a multilevel output voltage with minimum harmonic content (B. Wu, 2005). The equivalent switching frequency of the converter, f_{eq} is given by:

$$f_{eq} = Nf_{cr} \quad (1)$$

where f_{cr} is the carrier frequency.

The CPS-PWM technique provides equal conduction times for all the SMs (Konstantinou & Agelidis, 2009).

The modulation voltage is synthesized via high level VSC control comprising all the two cascaded control loops (average DC capacitor voltage balancing control, and individual DC capacitor voltage balancing control) taking into account the reference AC voltage command of the phase, v_{ac}^{*} while the DC supply voltage, V_{dc} is added as feedforward term.

The voltage commands, v_k^{*} for each SM in the upper arm is given by:

$$v_k^{*} = v_{avg\_up}^{*} + v_{bal}^{*} - \frac{v_{ac}^{*}}{N} + \frac{V_{dc}}{2N} \quad (k = 1{:}N) \quad (2)$$

while the voltage commands for each SM in the lower arm, v_k^{*} is given by:

$$v_k^{*} = v_{avg\_low}^{*} + v_{bal}^{*} + \frac{v_{ac}^{*}}{N} + \frac{V_{dc}}{2N} \; (k = N+1{:}2N) \quad (3)$$

where $v_{avg\_up}^{*}$ and $v_{avg\_low}^{*}$ are voltage command from the averaging control for the upper and lower arms respectively, v_{bal}^{*} is the voltage command from the individual voltage balancing control, v_{ac}^{*} is the the reference AC voltage command of the phase V_{dc} is the input DC voltage and N is the number of submodule per arm.

The value of v_k^{*} in each SM is normalized by the SM capacitor voltage, v_{Ck}. Each of the resulting modulating signals were individually compared with carrier signal of switching frequency, f_{cr}. To enhance current controllability and ensure harmonic cancellation, the carrier waveforms of the SM cells were phase shifted by $360^{o}/N$. Accordingly, multilevel voltage waveform with $N+1$ levels are obtained at each arm of the converter.

4. EXPERIMENTAL DEMONSTRATION

4.1. Experimental Setup

It is a well-known fact that modular multilevel converters are intended for high voltage high power applications such as HVDC systems. However, experimental implementation of such system requires huge resources in terms of software and hardware in addition to safety issues that have to be assessed in the laboratory. As such, a reduced order laboratory prototype is implemented as a proof of concept. The hardware prototype is shown in Figure 7 while Table 1 shows the component parameters.

The hardware is a single phase system with 4 SMs per arm with a DC link voltage of 100V. The main prerequisites for the experimental setup are:

- Four Farnell L30-5 “linear” 30V 5A power supply units (PSUs) for providing electrical interphase to the converter arms,
- DSP TMS320F28377D Dual-Core Delfino™ Microcontroller board,
- Two way eight drive circuit board for generating and sending the PWM signals to the SM/arm board capacitor voltage measurements,
- Nine LV 25-P voltage transducers for measuring SM capacitor voltages and the output voltage,
- Three CAS15-NP current transducers for measuring arm currents (upper and lower) and the output current.

Table 1: Parameters of the Experimental Set-up

Parameter	Value
Number of submodule per arm	4
Submodule capacitance	4.7mF
Reference capacitor voltage	25V
Arm inductance	1mH
Load resistor	5Ω
Load inductor	4mH
DC link voltage	100V
Output AC voltage reference	50V
Carrier frequency	4kHz
Modulation index	0.9

Figure 7: Experimental MMC Prototype

4.2. Sizing of Submodule Capacitor

The aim of the SM capacitor is to suppress the voltage fluctuations arising from the flow of arm current through the capacitor when the SM is inserted during operation. The SM capacitance used in the experiment was sized based on the following (Ilves, Norrga, Harnefors, & Nee, 2014):

$$C_{min} = \frac{2N \,.\, \Delta W_{max}}{(V_{dc}.\epsilon)2} \tag{4}$$

where ΔW_{max} is the maximum energy change in one SM, ϵ is the maximum voltage ripple, V_{dc} is the DC bus voltage, and N is the number of SM per arm.

4.3. Sizing of Arm Inductance

The aim of the arm inductor is to suppress the high frequency components of the arm current. The arm inductance used in the experiment was sized based on reducing the current ripple and limiting the fault current rise rate during fault as follows (Tu, Xu, Huang, & Zhang, 2010):

$$L_{arm} = \frac{V_{dc}}{2\alpha} \tag{5}$$

where α is the fault current rise rate.

5. RESULTS AND DISCUSSION

Experimental results are presented in this section to validate the design details and the control method. However, the voltage and current transducers were initially calibrated to ensure correct values are sent to the measurement unit.

As an initial test, the enhanced pulse width modulation signals (ePWMs) and SM capacitor voltages were probed.

Figure 8 and 9 show the ePWM signals in the upper and lower arm of the converter respectively. It is clear to see that the eight ePWM signals have a phase shift of 45° (=360°/8) to each other, this will guarantee harmonic reduction and enhance current controllability.

Figure 10 and 11 show the SM capacitor voltages in the upper and lower arm of the converter respectively. It is clear to see that the SM capacitor voltages were regulated to the reference value which confirms the effectiveness of the average DC capacitor voltage balancing control and the individual DC capacitor voltage balancing control.

Figure 12 and 13 show the multilevel voltage and current waveform of the upper arm of the converter respectively while Figure 14 and 15 show their equivalent in the lower arm of the converter. It can be seen that the multilevel arm voltages (Figure 12 and 14) show reduced harmonic content as required by HVDC transmission system. On the other hand, arm current waveforms (Figure 13 and 15) show second harmonic component. This is expected because of the uncontrolled circulating current in the converter. However, it is worth noticing that circulating current does manifest itself only in the internal dynamics of the converter. It does not affect the outer dynamics of the converter as can be seen in the output current waveform of the converter (Figure 17) which is of smooth sinusoidal waveform.

Figure 16 and 17 shows the staircase multilevel output voltage and current waveform of the converter. It can be seen that the output voltage (Figure 16) is nearly sinusoidal in shape with reduced harmonic content. This is a major requirement of HVDC transmission system. The output AC side current (Figure 17) is also of smooth sinusoidal waveform form free of harmonics and with improved quality, thus confirming the effectiveness of the MMC in HVDC transmission system.

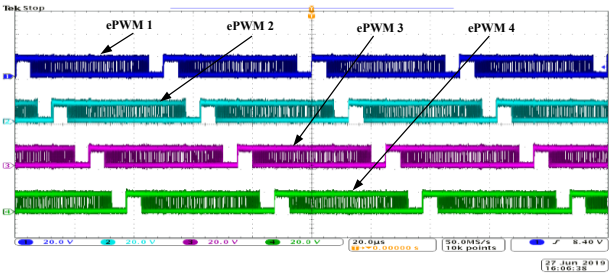

Figure 8: ePWM Signals for Upper Arm

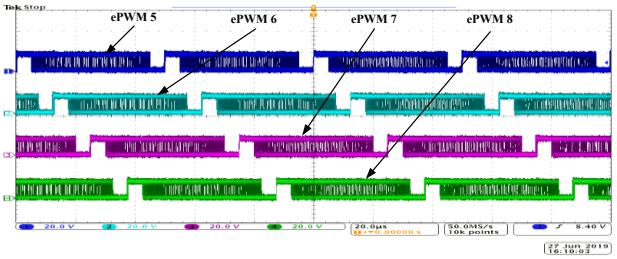

Figure 9: ePWM Signals for Lower Arm

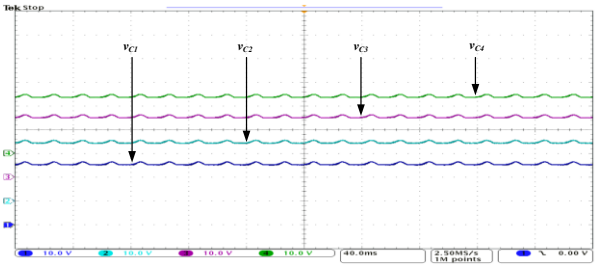

Figure 10: Submodule Capacitor Voltages for Upper Arm

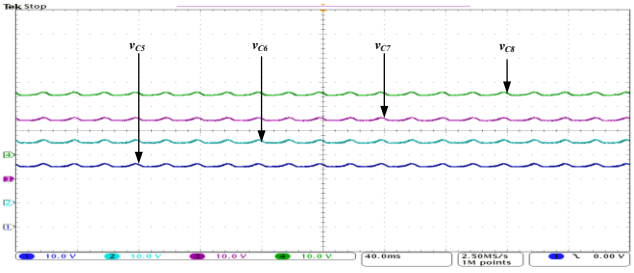

Figure 11: Submodule Capacitor Voltages for Lower Arm

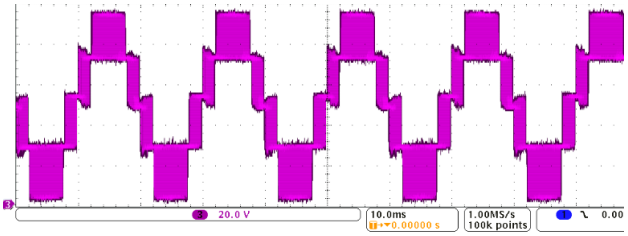

Figure 12: Upper Arm Voltage

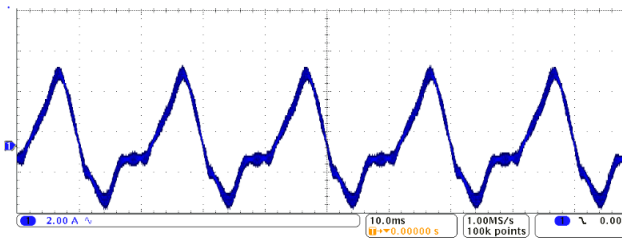

Figure 13: Upper Arm Current

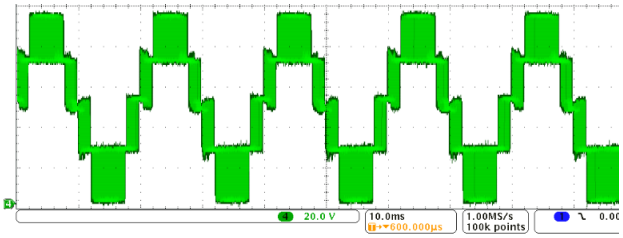

Figure 14: Lower Arm Voltage

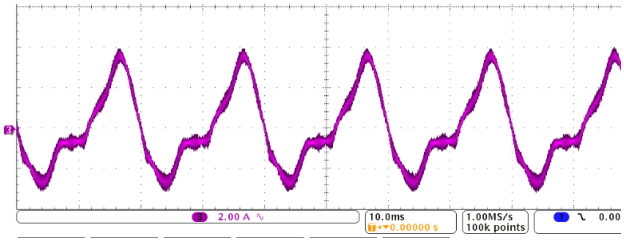

Figure 15: Lower Arm Current

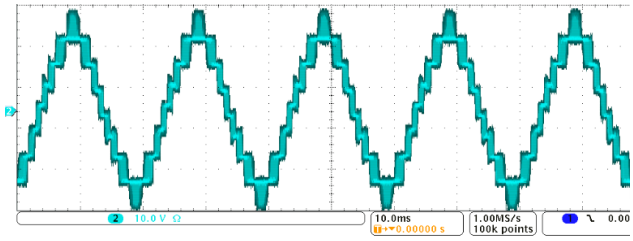

Figure 16: Output Voltage

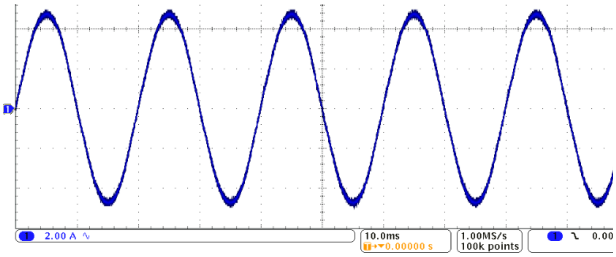

Figure 17: Output Current

6. CONCLUSION

Hardware and software implementation of reduced order laboratory prototype MMC have been presented for use in HVDC transmission system with a view of addressing the problems with the conventional two-level and three-level converters used previously. The hardware prototype was demonstrated on an MMC with four submodules per arm and the software aspect was implemented with TMS320F28377D Dual-Core Delfino™ Microcontroller board from Texas Instrument. Experimental results show that the MMC exhibits improved quality of the AC side current waveform with reduced harmonic distortion and staircase multilevel voltage waveform of nearly sinusoidal shape which could not be achieved by the conventional two-level and three-level converters, thus, demonstrating the effectiveness of MMC in HVDC transmission system.

REFERENCES

Abouelatta, M. A., Ward, S. A., Sayed, A. M., Mahmoud, K., Lehtonen, M., & Darwish, M. M. F. (2020). Fast Corona Discharge Assessment Using FDM Integrated With Full Multigrid Method in HVDC Transmission Lines Considering Wind Impact. *IEEE Access, Vol. 8*, pp. 225872-225883.

Adam, G. P., Abdelsalam, I., Fletcher, J. E., Burt, G. M., Holliday, D., & Finney, S. J. (2017). New Efficient

Submodule for a Modular Multilevel Converter in Multiterminal HVDC Networks. *IEEE Transactions on Power Electronics, Vol. 33, No. 6*, pp. 4258-4278.

Ahmed, N., Angquist, L., & mahmood, S. (2015). Efficient Modelling of an MMC-Based Multi-Terminal DC System Employing Hybrid HVDC Breakers. *IEEE Transactions on Power Delivery, Vol. 30, No. 4*, pp. 792-801.

Ansari, J. A., Liu, C., & Khan, S. A. (2020). MMC Based MTDC Grids: A Detailed Review on Issues and Challenges for Operation, Control and Protection Schemes. *IEEE Access, Vol. 8*, pp. 168154-168165

Beza, M., & Bongiorno, M. (2019). Identification of Resonance Interactions in Offshore-Wind Farms Connected to the Main Grid by MMC-Based HVDC System. *Electrical Power and Energy Systems, Vol. 111*, pp. 101-113.

Chen, X., Liu, J., Song, S., & Ouyang, S. (2020). Circulating Harmonic Currents Suppression of Level-Increased NLM Based Modular Multilevel Converter With Deadbeat Control. *IEEE Transactions on Power Electronics, Vol. 35, No. 11*, pp. 11418-11429.

Datasheet. DSP-TI TMS320F28377D. *http://www.ti.com/lit/ds/symlink/tms320f28377d-ep.pdf*.

Diez, C. M., Costabeber, A., Tardelli, F., Trainer, D., & Clare, J. (2020). Control and Experimental Validation of the Series Bridge Modular Multilevel Converter for HVDC Applications. *IEEE Transactions on Power Electronics, Vol. 35, No. 3*, pp. 2389-2401.

Elgamasy, M. M., Talaab, A. I., Kawady, T. A., Izzularab, M. A., & Elkalashy, N. I. (2020). Wave Propagation Differential Protection Scheme for VSC-HVDC Transmission Systems. *Electric Power Systems Research, Vol. 189*, pp. 1-10.

Elgeziry, M., Elsadd, M., Alkalashy, N., Kawady, T., Taalab, A., & Izzularab, M. A. (2019). Non-pilot protection scheme for multiterminal VSC–HVDC transmission systems. *IET Renewable Power Generation, Vol. 13, No. 16*, pp. 3033-3042.

Gonzalez-Torres, J. C., Damn, G., Costan, V., Benchaib, A., & Lamnabhi-Lagarrigue, F. (2020). Transient Stability of Power Systems with Embedded VSC-HVDC Links: Stability Margins Analysis and Control. *IET Generation, Transmission & Distribution, Vol. 14, No. 17*, 3pp. 377-3388.

Han, X., Sima, W., Yang, M., Li, L., Yuan, T., & Si, Y. (2018). Transient Characteristics Under Ground and Short-Circuit Faults in a ±500 kV MMC-Based HVDC System With Hybrid DC Circuit Breakers. *IEEE Transactions on Power Delivery, Vol. 33, No. 3*, pp. 1378-1387.

Hannan, M. A., Hussin, I., Hoque, M. M., Lipu, M. S. H., Hussain, A., Rahman, M. S. A., . . . Blaabjerg, F. (2018). Advanced Control Strategies of VSC Based HVDC Transmission System: Issues and Potential Recommendations. *IEEE Access, Vol. 6*, pp. 78352-78369.

Hao, Q., Li, Z., Gao, F., & Zhang, J. (2019). Reduced-Order Small-Signal Models of Modular Multilevel Converter and MMC-Based HVDC Grid. *IEEE Transactions on Industrial Electronics, Vol. 66, No. 3*, pp. 2257-2268.

Harnefors, L., Antonopoulos, A., Norrga, S., Angquist, L., & Nee, H. (2013). Dynamic Analysis of Modular Multilevel Converters. *IEEE Transactions on Industrial Electronics, Vol. 60, No. 7*, pp. 2526-2537.

Hu, J., Xu, K., Lin, L., & Zeng, R. (2017). Analysis and Enhanced Control of Hybrid-MMC-Based HVDC Systems During Asymmetrical DC Voltage Faults. *IEEE Transactions on Power Delivery, Vol. 33, No. 3*, 3pp. 94-403.

Ilves, K., Norrga, S., Harnefors, L., & Nee, H. (2014). On Energy Storage Requirements in Modular Multilevel Converters. *IEEE Transactions on Power Electronics, Vol. 29, No. 9*, pp. 77-88.

Jamshidifar, A., & Jovcic, D. (2015). Small-Signal Dynamic DQ Model of Modular Multilevel Converter for System Studies. *IEEE Trans. on Power Delivery, Vol. 31*, pp. 191-199.

Jiao, Y., & Nian, H. (2020). Grid-Forming Control for DFIG Based Wind Farms to Enhance the Stability of LCC-

HVDC. *IEEE Access, Vol. 8*, pp. 156752-156762.

Kadandani, N. B., Dahidah, M., & Ethni, S. (2021a). Design and Development of Modular Multilevel Converter for Solid State Transformer Application. *Bayero Journal of Engineering and Technology (BJET), Vol. 16, No. 1*, pp. 31-41.

Kadandani, N. B., Dahidah, M., & Ethni, S. (2021b). Review of Circulating Current Control Methods in Modular Multilevel Converter. *Bayero Journal of Engineering and Technology (BJET), Vol. 16, No. 1*, pp. 62-75.

Khazaei, J., Idowu, P., Asrari, A., Shafaye, A. B., & Piyasinghe, L. (2020). Review of HVDC control in weak AC grids. *Electric Power Systems Research, Vol. 162*, pp. 194-206.

Konstantinou, G. S., & Agelidis, V. G. (2009). Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques. *2009 4th IEEE Conference on Industrial Electronics and Applications, Xi'an*, pp. 3399-3404.

Lesnicar, A., & R.Marquardt. (2003). An Innovative Modular Multilevel Converter Topology Suitable for a Wide Power Range. *Proceedings of IEEE Power Tech Conference, pp. 1-* 6.

Luan, K., Li, Y., Li, Z., Zhao, C., Xu, F., Gao, F., & Wang, P. (2019). Analysis and Design of PWM-CSC for HVDC Transmission Systems. *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal*, pp. 4773-4777.

Marquardt, R. (2002). Current Rectification Circuit for Voltage Source Inverters with Separate Energy Stores Replaces Phase Blocks with Energy Storing Capacitors. *German Patent (DE10103031A1)*.

Pérez-Basante, A., Ceballos, S., Konstantinou, G., Pou, J., Sanchen-Ruiz, A., Lopez, I., & Alegría, J. m. d. (2020). Circulating Current Control for Modular Multilevel Converters with (N+1) Selective Harmonic Elimination PWM *IEEE Transactions on Power Electronics, Vol. 35, No. 8*, pp. 712-725.

Sánchez-Sánchez, E., Prieto-Araujo, E., Junyent-Ferré, A., & Gomis-Bellmunt, O. (2018). Analysis of MMC Energy-Based Control Structures for VSC-HVDC Links. *IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 6, No. 3*, pp. 1065-1076.

Schönleber, K., Oudalov, A., Krontiris, A., & Lundberg, P. (2020). Opportunities for Embedded High-Voltage Direct Current. *IEEE Power & Energy Magazine*, pp. 58-63.

Shi, X., Filizadeh, S., & Jacobson, D. A. (2018). Loss Evaluation for the Hybrid Cascaded MMC Under Different Voltage-Regulation Methods. *IEEE Transactions on Energy Conversion, Vol. 33, No. 3*, pp. 1487-1498.

Tanta, M., Pinto, J. G., Monteiro, V., Martins, A. P., Carvalho, A. S., & Afonso, J. L. (2020). Deadbeat Predictive Current Control for Circulating Currents Reduction in a Modular Multilevel Converter Based Rail Power Conditioner. *Applied Science, Vol. 10*, pp. 1-22.

Teng, Y., & Li, X. (2020). Improved Approach to High-Frequency Current Injection-Based Protection for Grounding Electrode Line in High-Voltage Direct Current System. *IEEE Transactions on Industry Applications, Vol. 56, No. 3*, pp. 2409-2417.

Tu, Q., Xu, Z., Huang, H., & Zhang, J. (2010). Parameter design principle of the arm inductor in modular multilevel converter based HVDC. *Proceedings of International Conference on Power System Technology (POWERCON)*, pp. 1-6.

Wang, L., Yang, Z., Lu, X., & Prokhorov, A. (2017). Stability Analysis of a Hybrid Multi-Infeed HVDC System Connected Between Two Offshore Wind Farms and Two Power Grids. *IEEE Transactions on Industry Applications, Vol. 53, No. 3*, pp. 1824–1833.

Wang, Y., Wen, W., Wang, C., Liu, H., Zhan, X., & Xiao, X. (2019). Adaptive Voltage Droop Method of Multiterminal VSC-HVDC Systems for DC Voltage Deviation and Power Sharing. *IEEE Transactions on Power Delivery, Vol. 34, No. 1*, pp. 169-176.

Wu, B. (2005). High Power Converters and AC Drives. *New York: IEEE Press/Wiley*.

Wu, H., Liu, Y., Wang, Z., Song, L., & Wu, F. (2019). Flexible CSC-HVDC System. *IET Journal of Engineering, Vol.*

2019, No. 16, pp. 2337-2342.

Wu, W., Chen, Y., Zhou, L., Zhou, X., Yang, L., Dong, Y., . . . Luo, A. (2018). A Virtual Phase-Lead Impedance Stability Control Strategy for the Maritime VSC–HVDC System. *IEEE Transaction on Industrial Electronics, Vol. 14, No. 12*, pp. 5475-5488.

Ye, Y., Lu, Z., Xie, L., & Qiao, Y. (2018). A Coordinated Frequency Regulation Strategy for VSC-HVDC Integrated Offshore Wind Farms. *Proceedings of IEEE Power Energy Soiety General Meeting*.

Zhang, Y., Klabunde, C., & Wolter, M. (2020). Frequency-Coupled Impedance Modeling and Resonance Analysis of DFIG-Based Offshore Wind Farm With HVDC Connection. *IEEE Access, Vol. 8*, pp. 147880-147894.

Zhu, R., Lin, N., Dinavahi, V., & Liang, G. (2020). An Accurate and Fast Method for Conducted EMI Modeling and Simulation of MMC-Based HVDC Converter Station. *IEEE Transactions on Power Electronics, Vol. 35, No. 5*, pp. 4689-4702.